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S5200D

DIGITAL TRANSMISSION TEST TRANSMITTER

USER MANUAL

FORM 0160-0982D

tau-tron

A UNIT OF

GENERAL SIGNAL

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S5200D

DIGITAL TRANSMISSION TEST TRANSMITTER

USER MANUAL
FORM 0160-0982D

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Phone (617)692-5100 Telex 750245 1-800-TAU-TRON (Outside MA)

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If there are signs of damage on the outside of the carton or in the cushioning material, it should be kept until the instrument has been checked mechanically and electrically.

Procedures for checking electrical performance are found in Section 6. If there is mechanical damage or defect, or if the performance fails to meet specifications, notify the factory and follow the procedures outlined under Repair Returns in Section 8.

SAFETY INFORMATION

CAUTION

This instrument may be damaged if operated with the Line Voltage Selector or the rear-panel AC connector set for the wrong applied line voltage. (see Power, 2.2)

This instrument is designed to operate from a single phase power source, with one of the current carrying conductors at ground. Operation from power sources where both current carrying conductors are live with respect to ground is not recommended.

WARNING

To avoid dangerous electrical shock, do not perform electrical tasks when there are signs of shipping damage to any part of the instrument case.

WARNING

Before the instrument is switched on, all protective ground terminals, extension cords, autotransformers and devices connected to it should be connected to a protective grounded socket. Any interruption of the protective grounding will cause a potential shock hazard that could result in personal injury.

CAUTION

Cautions regarding AC power sources used with this instrument are not solely for safety purposes. This instrument will not power-up properly unless the power receptacle is grounded, and hot and neutral conductors are properly connected in the receptacle. Usual symptoms are:

1) Three error indicators lighting simultaneously.
2) Display is blank.

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Section 1, Introduction

1.1 SCOPE

This manual provides operation, testing applications, performance, interfacing, theory of operation, and basic diagnostic information for the Tau-Tron S5200D Digital Transmission Test Set Transmitter.

1.2 DESCRIPTION

The Tau-Tron S5200D Digital Transmission Test Transmitter together with its companion instrument, the S5200D Digital Transmission Test Receiver, form a compact test set for detailed measurements of systems operating at the DS3 transmission rate.

The S5200D transmitter has six bipolar outputs and binary data plus clock NRZ outputs. Bipolar outputs can be set to any of three levels including DSX-3. Four output patterns are available; the Bell standard pseudorandom bit sequence and three short data patterns. DS3 framed and unframed formats for all data patterns are also selectable. Internally generated transmission errors over a broad range from 10^{-2} to 10^{-9} are developed in a unique aperiodic way to assure an even statistical distribution of errors over all output bits. Other error-rates can be set using the external error-rate or external error burst modes.

Testing versatility is also enhanced thru DC operating capability and by the IEEE-488 (GPIB) interface for remote control. A review of the S5200D transmitter specifications will acquaint the user with complete features.

1.3 SPECIFICATIONS

INTERNAL CLOCK	Frequency	44.736MHz ±20ppm
EXTERNAL CLOCK	Frequency	44.736MHz ±3MHz
	Level	AC coupled, 800MV peak-to-peak minimum
	Impedance	75ohm source
	Connector	BNC, rear panel
DATA PATTERNS	PRBS	Repeating pseudorandom bit sequence of 2^{15}-1= 32767 bits
	Short Patterns	All one's Alternating 1100 Alternating 1010
	Blue Signal	DS3 Framed 1010 repeating sequence; logical one data bit follows frame bit.
FRAMING	Framed	Bell Compatible DS3 framing format
	Unframed	No framing bits, data pattern output only
BIPOLAR	Coding	Bipolar with 3 zero substitution (B3ZS)
	Level	
	High Output	0.91V peak nominal
	Low Output	13.8dB below nominal High, 0.186V peak nominal
	DSX Output	High output passed through equivalent of 450 feet of 728A cable, typically 5 to 6dB below High, 0.48V peak typical
	Impedance	75ohm source
	Connector	WECo 358
	Quantity	6 identical outputs
BINARY DATA & CLOCK OUTPUTS	Coding	Non return to zero (NRZ)
	Level	Logic one = +1V Logic zero = -1V (into 75ohm load)
	Phasing	Rising clock edge in center of data ±4ns
	Impedance	75ohm source
	Connector	BNC

ERROR INJECTION	Internal Error	
	General	Error-rate injection on output signal over all bits. In unframed mode errors are on data bits. In framed mode errors are in data and DS3 framing bits affecting both bit and parity.
	Method	Aperiodic insertion to insure even statistical error distribution over all bits.
	Rate	1×10^{-N} for N=2 thru 9 in increments of 1.
	Single Errors	Single bit or single bipolar violation
	External Error	
	General	External bit errors inserted by applying external generator. In rate mode, errors are proportional to frequency. In burst mode, errors occur during positive cycle of external input.
	External Level	TTL level
	Impedance	300ohm source
	Rate	Any error-rate less then approximately 450K errors/sec.
	Burst	100% errors during positive portion of waveform. 10 bit error burst minimum.
MONITOR	Outputs	PRBS Sync, pseudorandom data pattern sync M-Sync, DS3 frame sync Power fail latching indication of previous lost AC or DC power.
	Input	X-Bit TTL low or ground to change X-Bit from normal logic 1 to 0.
	Level	TTL compatible
	Interface	24-pin D-Connector, rear panel
POWER	AC	115VAC, 50 to 60HZ, 60VA maximum
	DC Option 08	-21 to -27VDC or -42 to -54VDC, 90VA maximum.
MECHANICAL	Dimension	6.6 in. high x 13.6 in. wide x 19.8 in. deep.
	Weight	19lb. net, 24lb. shipping

1.4 OPTIONS AVAILABLE

Binary Output,	OP-01	Consult factory for optional TTL or ECL compatible outputs.
IEEE-488 Interface (GPIB)	OP-02	As defined in IEEE Std 488-1978, the following GPIB capabilities are implemented:

SH1 Complete source handshake.
AH1 Complete accepter handshake.
T6 Basic talker, serial poll, no talk only, unaddressed if addressed to listen.
TE0 No extended talker (secondary talk address) capability.
L3 Basic listener, listen only, unaddress if addressed to talk.
LE0 No extended listener (secondary listen address) capability.
SR1 Complete service request capability.
RL2 No local lockout on remote/local capability.
PP0 No parallel poll capablity.
DC1 Complete device clear capability.
DT1 Complete device trigger capability.
C0 No control capability.
E2 Tri-state drivers are used on DIO lines to achieve maximum data transfer rates.

All S5200D transmitter functions controllable from the front panel may be remotely controlled. Transmitter status may be accessed by a GPIB controller.

DC POWER,	OP-08	Interval DC input capability -21 to -27VDC or -42 to -54VDC 90VA maximum, 6.25A slow-blow fuse. Unit can be powered from AC only, DC only or if AC and DC are simultaneously applied, unit will operate from AC until AC is off and then automatically switches to DC. Included with option 08 is a DC power cord.

1.5 ACCESSORIES

Accessories Supplied	AC Power Cord	3-wire grounded cord
	Spare AC Fuse	2 A slow-blow
	Mating D-Connector	For rear-panel monitor connector
	Protective Front Cover	
	Instruction Manual	

Accessories Available	S5201-1	Hard Shell Shipping Case 11 in. high x 18 in. wide x 23.5 in. long
	S5201-2	Soft Carrying Case 16 in. high x 8.5 in. wide x 22 in. long
	S5201-4	Rackmount Kit, 8.75 in. high x 19 in. wide x 18.5 in. long.

Section 2, Installation

2.1 SITE REQUIREMENTS

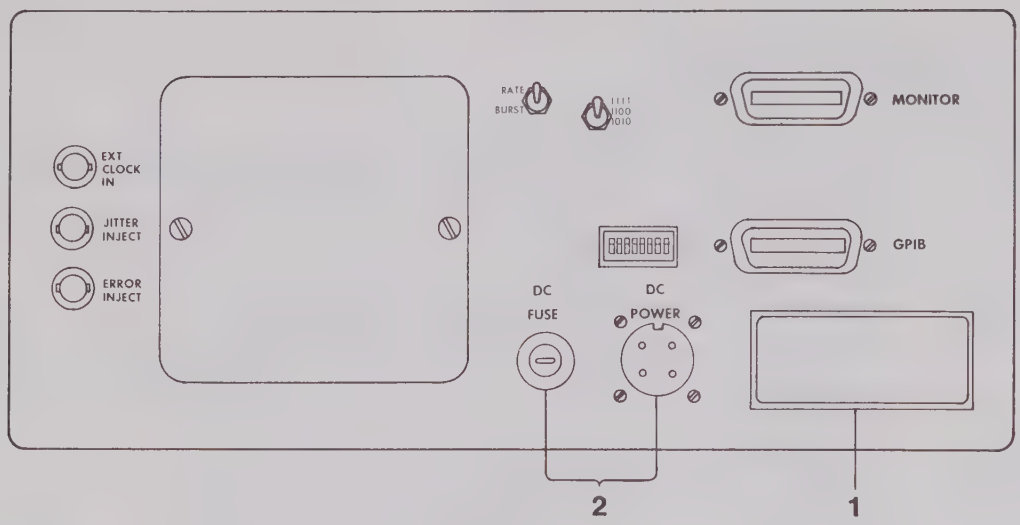
AC Power	115V ±10%, 50 to 60Hz, 60VA.
DC Power	With Option-08 DC Power only; -21 to -27V or -42 to -54VDC, 90VA. (4A at -24V, 2A at -48V)
Temperature	32 to 104°F (0 to 40°C).
Humidity	0 to 95% RH max at 20°C, non-condensing.
Size	13.6 in. wide x 19.8 in. deep x 6.6 in. high overall including cover, handle, and rubber feet.
Weight	19 lb. net.
Clearances	3 in. behind and 1 in. above and below.

CAUTION

Cautions regarding AC power sources used with this instrument are not solely for safety purposes. This instrument will not power-up properly unless the power receptacle is grounded, and hot and neutral conductors are properly connected in the receptacle. Usual symptoms are:

1) Three error indicators lighting simultaneously.
2) Display is blank.

2.2 POWER



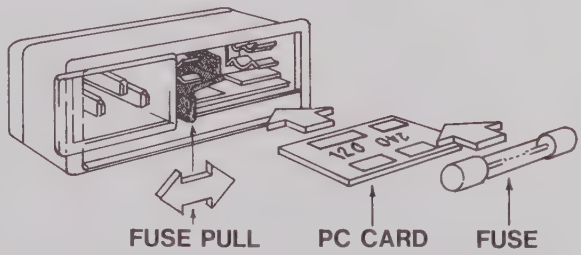
CAUTION Be sure the line-voltage selector in the rear-panel AC connector is set for 120V before connecting to the AC line. If the incorrect range is selected, the unit could be damaged. It is also necessary to use a three-wire grounded circuit.

1. AC Power Three-wire connector accepts the 6-foot power cord supplied. Before connection, check that the 120V line-voltage range is selected and proper fuse is installed:

a. Slide cover down to left and push FUSE PULL To the left.

b. Remove fuse and check that it is a 2A slo-blo.

c. Check that the legend on the PC card in the connector reads 120V. (The card is also marked for 240V, 100V, and 220V but these ranges are not available on this unit). If it doesn't, remove the card (pull straight out), turn it around, and reinsert.



d. Rotate FUSE PULL back into its normal position and reinstall the fuse.

CAUTION Do not exceed -54VDC input. If the input exceeds -54V, the DC FUSE will blow or the internal DC supply will cease functioning.

2. DC Power OP-08 Only

A DC POWER input connector and a DC FUSE holder are installed on all units but are functional only with those shipped with Option 08 DC Power. The connector is a 4-pin jack for -21 to -27V or -42 to -54VDC office-battery power and is for use with the 6-foot detachable power cord supplied. The fuse is 6.25A slo-blo.

Unit can be powered from AC only, DC only or if AC and DC are simultaneously applied, unit will operate from AC until AC is off and then automatically switch to DC.

Pin assignments are as follows:

A and B - GND
C and D - -VDC

The mating connector is Amphenol 14S-2SF.

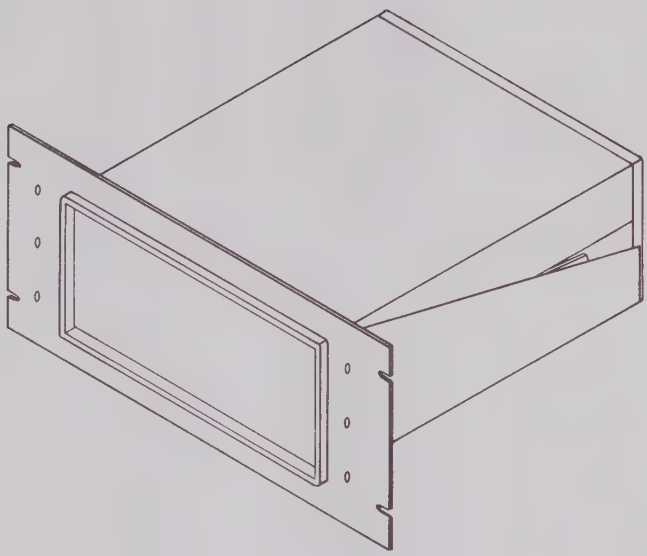
2.3 RACKMOUNTING

The unit can be rackmounted on a standard 19 in. rack by means of an S5201-4 (Rackmount Kit). Panel height is 8.75 in. and depth behind panel is 18.5 in.

a. Remove the front 2 screws from the top and bottom covers of the unit.

b. Slide the rackmount panel from the kit over the front of the unit and attach with the screws removed in step a.

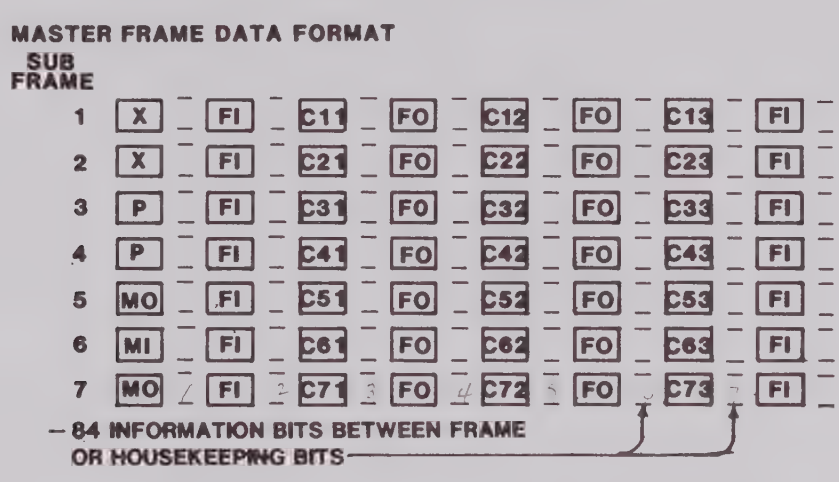
c. Mount the unit in the rack. Be sure clearances of 3 in. and 1 in. above and below are allowed.



Section 3, DS3 Testing

3.1 DS3 SIGNAL FORMAT

The 44.736 Mb/s DS3 signal format generated by the S5200D transmitter, MX3 and other multiplexers provide the basis for all DS3 framed measurements. Parity measurements on live traffic signals are made utilizing the DS3 format shown in the figure.


MASTER FRAME DATA FORMAT
SUB FRAME
1 X FI C11 FO C12 FO C13 FI
2 X FI C21 FO C22 FO C23 FI
3 P FI C31 FO C32 FO C33 FI
4 P FI C41 FO C42 FO C43 FI
5 MO FI C51 FO C52 FO C53 FI
6 MI FI C61 FO C62 FO C63 FI
7 MO FI C71 FO C72 FO C73 FI
– 84 INFORMATION BITS BETWEEN FRAME OR HOUSEKEEPING BITS

- M FRAME IS ALL 56 FRAME BITS AND 4704 INFORMATION BITS, TOTAL 4760 BITS,
- FRAME ALIGNMENT SIGNAL IS FI = 1, FO = 0.
- MULTI-FRAME ALIGNMENT SIGNAL IS MO,MI,MO (MO = 0,MI = 1).
- PARITY INFORMATION IS PP AND IS TAKEN OVER ALL INFORMATION BITS IN THE PRECEDING M FRAME PP = 1 IF THE SUM OF ALL INFORMATION BITS IS 1, PP = 0 IF THE SUM IS 0.
- ALARM SERVICE CHANNEL IS XX. IN ANY ONE M FRAME THE TWO X-BITS MUST BE IDENTICAL.
- STUFFING INDICATOR WORD IS THE C-BITS.
- INFORMATION BITS WITH S5200D-TX CAN BE $2^{15}-1$ PSEUDORANDOM SEQUENCE . WITH LIVE TRAFFIC IT IS SEVEN 6.312 MB/S DATA SOURCES.

There are 7 Subframes in the Master, or M Frame, each subframe consists of 8 groups of 1 housekeeping bit and 84 information bits.

The groups of 84 information bits can consist of sequences such as pseudorandom bit sequences (PRBS) or short repeating bit sequences generated by test sets, or system information such as live traffic or patterns such as "Blue Signal" codes. When live traffic is being transmitted, the 84 data bits consist of seven DS2 signals sampled twelve times. The 6.312Mb/s DS2 signal is made of four 1.544Mb/s DS1 signals. The DS1 signal can contain 24 PCM encoded voice channels, so a complete DS3 signal can contain 24x4x7=672 voice channels.

The DS3 housekeeping bits, occurring once every 85 bits, serve a variety of purposes. The 2nd, 4th, 6th and 8th housekeeping bit in each subframe is termed the F-bit or Frame Alignment signal. This four-bit sequence of F1, F0, F0, F1=1001 is identical for each subframe. This known, repeating sequence is searched for and located by demultiplexing or test equipment so that the positions of the 84 information bits and housekeeping bits can be determined.

Demultiplexing or test equipment circuitry then must locate the seven subframes. The Marker bits or M-bits are a sequence of M0, M1, M0=010 in the fifth, sixth and seventh subframe of each Master Frame which serves this purpose. The method of locating the F and M-bits is determined by the framing algorithm used in the communications equipment and is an important parameter in any system. The time to acquire DS3 Frame synchronization depends on the algorithm used and typically takes from 2 to 3 milliseconds.

Once the subframes are located, the seven stuffing indicator words corresponding to the seven multiplexed DS2 channels are known. These 3-bit words (C11, C12, C13 in subframe 1) are always all zeros or all ones indicating the absence or presence of stuffing bits necessary for the asynchronous multiplexing and demultiplexing of the DS2 channels.

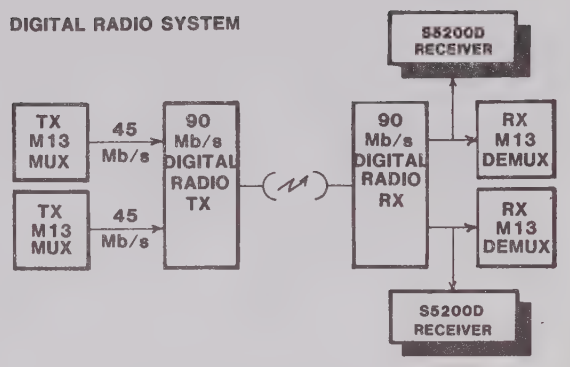
Subframe location also defines the Parity (or P-bit) and X-bit locations. The P-bits in a Master Frame are used to provide a measure of error performance in the previous Master Frame. If the digital modulo-2 sum of all 7x8x84 = 4704 information bits in a Master Frame is 1 then PP=11 is output by the multiplexing or transmitting equipment in the next Master Frame. If the sum is 0 then PP=00 is output. The demultiplexing equipment or test set receiver counts the 4704 information bits in the Master Frame and compares this sum to the PP bits in the incoming format. If a transmission error has occurred in the information bits, the PP will not compare. The parity bits can be used to detect transmission errors in live traffic; however, if the error-rate is such that double or even numbers of errors occur in a Master Frame, the parity error measuring becomes invalid. This occurs at error-rates worse than $1/4704 = 2.1 \times 10^{-4}$.

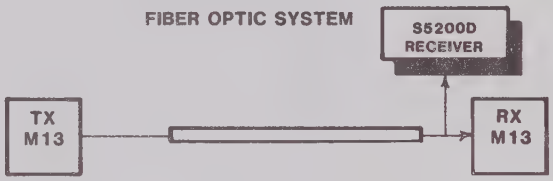
The X-bits are not defined by present DS3 specifications but are normally 1, 1 and must be identical, just as the P-bits are, in a Master Frame. This requirement aids the search for the M-bits. The X-bits are used in some systems as an alarm or control channel. The S5200D receiver provides an X-bit output which can be used to log occurrences in a particular system. The X-bit input of the S5200D transmitter can be used with the receiver X-bit output to provide an auxiliary information channel. The X-bit rate is approximately 9.4kb/s.

3.2 PARITY ERROR TESTING

Use

The parity-error mode is used to measure live traffic on standard data-format DS3 signals generated by MX3 or M13 multiplexers. Parity measurements can be made on single hops or multi-hops if the parity is not restored at each repeater in the multi-hop system.





Parity Code

The multiplexer counts all the information bits in one Master Frame of 4760 bits. If the digital sum of all 4704 information bits is 1 then PP=11 in the next Master Frame. If the sum is 0 then PP=00 in the next Master Frame.

Parity Measurement

The S5200D receiver monitors the DS3 signal at the receive end of the transmission system, finds frame, and counts all of the 4704 information bits in the Master Frame. It then compares the digital sum to the PP bits in the incoming format and, if they do not agree, generates a parity error.

MASTER FRAME DATA FORMAT

SUB FRAME														
1	X	FI	C11	FO	C12	FO	C13	FI						
2	X	FI	C21	FO	C22	FO	C23	FI						
3	P	FI	C31	FO	C32	FO	C33	FI						
4	P	FI	C41	FO	C42	FO	C43	FI						
5	MO	FI	C51	FO	C52	FO	C53	FI						
6	MI	FI	C61	FO	C62	FO	C63	FI						
7	MO	FI	C71	FO	C72	FO	C73	FI						

– 84 INFORMATION BITS BETWEEN FRAME OR HOUSEKEEPING BITS

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Even Number of Errors

At the transmitter, if the digital sum is 1 and one bit error is made in one detected Master Frame during transmission, the digital sum at the receiver will be 0 for that Master Frame and one parity error will be generated. Any odd number of bit errors (1,3,5,etc.) made in one Master Frame during transmission will be detected at the receiver as one parity error. Any even number of bit errors (2, 4, 6, etc.) made in one Master Frame during transmission will not be detected at the receiver.

Parity Errors vs. Bit Errors

The even/odd information from one frame is stored and compared to the parity bit received in the next frame. A difference indicates at least one data bit was in error. In general, the parity error-rate will track the bit error-rate but is limited to representing one data bit error in a frame (1 error bit divided by 4704 data bits= 2.1×10^{-4} error-rate). Thus, for error-rates greater than this, bit errors will often be greater than parity errors.

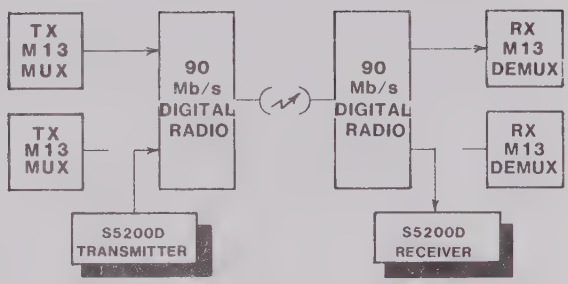
Error Multiplication Factor

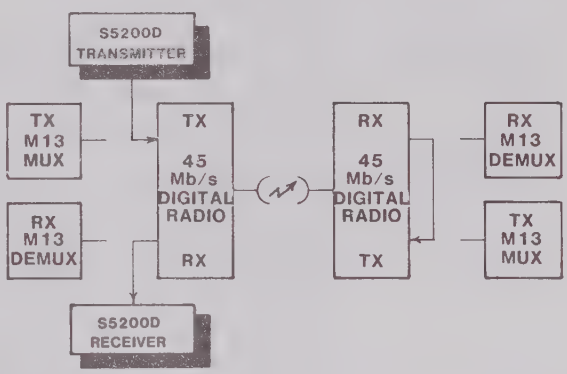
Most designers of digital systems use scramblers and descramblers and/or modulation schemes that cause a multiplication effect. This effect may result in three or more received errors from a single transmitted error. Fortunately, the error multiplication effect typically is contained within the 4704-bit frame. Usually system designers have made assurances that a statistically defined number of odd error sequences will occur so that the parity will still reflect bit errors. System manufacturers can supply the error multiplication factor for any particular system to allow the effective bit error-rate to be determined by measuring the parity error-rate.

3.3 BIT ERROR TESTING

Use

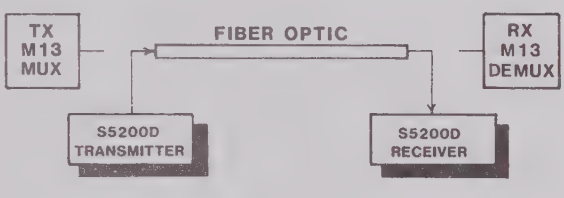
Bit-error measurements are usually made during the initial installation of digital transmission systems. They are made using either the 2^{15}-1 (32,767) bit pseudorandom pattern or short patterns generated by an S5200D transmitter. Bit measurements can be made in the framed or unframed mode, depending on system requirements.





Test Patterns

Bit error test equipment utilizes pseudorandom binary sequences or short patterns as the test pattern. The PRBS sequences, also sometimes called quasi-random sequences, are easily generated using digital shift register techniques. Their properties are such that the patterns appear to be random in nature. That is, the density of 1's and 0's in the sequence are approximately equal. Another characteristic of these sequences is that they do repeat after some number of bits. The formula which defines the length of the sequence in terms of its number of bits is given as 2^{n-1}, where n is the number of stages in the shift register generating the sequence. In the case of the S5200D, the number n equals 15 and therefore the length of the psuedormandom binary sequence before it repeats is 32,767 bits. Since the sequences do repeat, it is easy to synchronize an incoming sequence received by a receiver with a locally generated version of that same sequence.



Bit Measurements

The S5200D transmitter output is applied to the transmit end of the system and the S5200D receiver is connected to the receive end. The receiver synchronizes to the incoming pattern and compares it, bit-by-bit, to its own internal pseudorandom generator reference pattern. Any difference is counted as an error.

For systems not carrying live traffic, bit error measurements provide the most accurate assessment of system performance; however, with bit testing, several configurations are possible. Some parts of the systems do not require the DS3 format to operate properly. Inputs and outputs to some digital radio and fiber optic systems often only require the 44.736Mb/s DS3 rate and do not require framing bits. For these situations it may be desirable to utilize the unframed mode of the test set to eliminate the DS3 frame acquisition time of the receiver. This could be useful when checking hot standby switching times by observing the number of errors. For example, short patterns can be used in bit testing and a comparison of system performance between pseudorandom and short patterns can often be used in some systems to detect misalignment problems or timing recovery problems.

3.4 BIPOLAR-PULSE-VIOLATION (BPV) TESTING

Bipolar-Pulse-Violation (BPV) testing is valid for live traffic testing of cable systems and entrance links even though this type of testing has limited usefulness for DS3 systems.

The DS3 signal has a bipolar signal format. This means that all binary logical zeroes are transmitted as a OV signal and all binary logical ones are transmitted as positive or negative pulses of width equal to ½ the clock period. Bipolar coding requires that these pulses alternate in polarity. A noise impulse on a cable system or entrance link may cause a OV logical zero to be recognized as a bipolar pulse or may cause a legitimate bipolar pulse to be recognized as a OV logical zero. Either impairment will result in received bipolar pulses that do not alternate in polarity but that are of the same polarity. In this way, a performance determination can be made on a signal with a bipolar format without regard for data content or framing format.

The DS3 signal coding also requires a Bipolar 3 Zero Substitution (B3ZS) code. When 3 zeros are present in the binary data, substitution codes consisting, in part, of a bipolar violation are transmitted instead. The codes are varied to maintain the OV average DC level of the bipolar signal and are transmitted to guarantee activity on the line since some minimal activity is a requirement of some regenerative repeaters and some DS3 terminating equipment. This B3ZS coding makes BPV error measurements slightly more complex in that legitimate violation codes are not recorded as errors.

The S5200D receiver is excellent for BPV error measurements with its high input sensitivity and cable equalization optimized for 450 feet to 900 feet of 728A cable. BPV measurements of the DS3 signal have limited usefulness, however. Since the DS3 format includes a parity check, live traffic parity measurements are usually used. When bipolar pulses are passed through digital processing circuitry, the bipolar pulses are converted to binary logic levels and then processed. When these binary levels are then converted back to bipolar signals, any input bipolar violations are lost and not retransmitted. Thus BPV measurements can only be used to test a single section of a system. Where the DS3 framing format is available, parity measurements often provide more useful results.

3.5 SYSTEM CHARACTERIZATION USING ERROR SECONDS

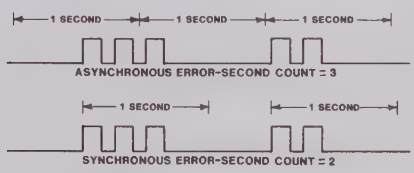
Synchronous Error Seconds

One measurement accepted as an indicator of performance is the error-second, defined as a one second period in which there are one or more errors. Specified limits for error-seconds are a requirement for some systems. Error-seconds have been used to compare systems and evaluate the effects of various parameters on system performance. In some instances the error-second measurement has been quantified by its severity. That is, if an error-second occurs in which the errors exceed a specified number, then it is recorded as a threshold error-second. In voice grade PCM systems, error-rates exceeding 10^{-6} error bits are sometimes of interest because the error perturbations become noticable at this error-rate. At 10^{-3} error-rates voice quality becomes unacceptable. As a result, 10^{-6} and 10^{-3} threshold error-seconds would be useful for assessing performance of systems accomodating voice PCM signals.

Tau-Tron has pioneered a new way of measuring these parameters, termed the synchronous error-second measurement, that has been shown to give more consistent and accurate results useful in analysis and diagnostic measurements.

A Note About Error-Second Measurements

Two types of error-second measurements are in general use, asynchronous and synchronous.



With asynchronous measurements, contiguous one-second measurements are made starting at some time independent of the errors. Any error or errors occurring during any one-second interval registers as an error-second. With synchronous measurements, the one-second measurements are triggered by the errors.

Synchronous errored-second measurements always give the lowest possible count and always give consistent counts - two test sets making the same measurement will always read the same. For these reasons they are preferred by industry and are the type used by Tau-Tron.

System Characterization

At first approximation, many digital systems can be characterized as having a combination of randomly distributed, infrequent, or dribbling type errors and occa-

sional error bursts. While all errors contribute to the overall, or average error-rate of a system, the causes of burst and dribbling errors are often quite different and quantifying these different types of errors and correlating them with other parameters can be very useful in determining their causes. Error bursts are caused by many things from power surges and propagation phenomena to intermittent connections and slamming doors; while dribbling type errors can often be related to system distortions, circuit misalignments, and other more subtle problems.

Dribbling errors, or errors that occur infrequently can be related to a system's error-rate "floor". This floor can be described as the best or lowest error-rate that a system achieves over a long period of time. Systems operating poorly may have a lower limit or error-rate floor of 1 error in 10^5 bits, or 10^{-5} error-rate. Systems operating properly may run for days without errors and have error-rate floors of 10^{-13}, 10^{-14} or even lower. In many cases the error-rate floor may be so low that it appears to be zero. The S5200D separates dribbling errors from other burst type errors and calculates a dribbling error-rate from these errors and the elapsed time of test to give an indication of the system's present error-rate floor, if burst type errors could be eliminated. One approach to system maintenance and trouble shooting is to attack the burst type error first since they may tend to mask the lower level dribbling errors. The S5200D also quantifies the severity of the burst errors and provides a correlation between other system parameters to aid in isolating cause and effect.

Threshold Error Seconds

Since the S5200D measures error-seconds sysnchronously, it can accurately quantify the error distribution of a system by an extension of the synchronous error-second to the synchronous threshold error-second. A threshold error-second is a second in which the error-rate exceeded a specific threshold. The S5200D simultaneously measures, in addition to other parameters, the number of error-seconds in which the error-rate exceeds 10^{-3}, 10^{-4}, 10^{-5} and 10^{-6}. In this way, a system can be characterized by the severity of error bursts that cause the specific thresholds to be exceeded. These specific error thresholds have been programmed into the solid-state memory of the S5200D and if the number of errors exceeds this threshold during an error-second, then the appropriate threshold error-second totals are incremented.

Thresholds

The number of errors that causes a specific error-rate depends on the mode of operation. For example, bit error measurements in the unframed mode are made on a bit-by-bit basis over all bits in the 44.736×10^6 bit per second data stream. An error-rate worse than 10^{-3} would then require more than 44,736 errors a second. Bit measurements in the framed mode are only made for the data bits and don't include the DS3 framing bits. The framing bits occur once every 85 bits so the effective data bit rate is 84/85 x 44.736Mb/s, or 44.210Mb/s. Thus, for the framed mode, the number of bit errors must exceed 44,210 errors in a second to cause an error-rate worse than 10^{-3}.

Parity measurement thresholds are the same as DS3 framed bit measurements with the exception that since the parity bit represents 4704 data bits in a DS3 Master Frame, the parity measurement cannot accurately detect error-rates worse than 1 error per 4704 bits or 2.1×10^{-4}. Thus, 10^{-3} threshold error-seconds are invalid. A 10^{-4} threshold parity error-second would require 4421 or more errors a second.

The error-second thresholds in the S5200D have been set to consider the mode of operation and have also been adjusted to take into account the accuracy of the internal crystal controlled timing circuit which generates the synchronous one second interval. The actual error thresholds for the specific threshold error-seconds are shown below:

ERROR THRESHOLDS IN ONE SECOND PERIOD		THRESHOLD ERROR RATE
DS3 Framed Mode Bit, Parity Measurement	Unframed Mode Bit Measurements	
≥44,100	≥44,700	1×10^{-3}
≥4,410	≥4,470	1×10^{-4}
≥441	≥447	1×10^{-5}
≥44	≥44	1×10^{-6}

If these error thresholds are exceeded, then the appropriate threshold error-second counts are incremented in the S5200D.

Dribbling Errors

When errors occur during a second that do not exceed a 10^{-6} error-rate, they are termed dribbling or residual errors. The S5200D receiver maintains an exact

totalized count of all dribbling errors and also calculates the dribbling error-rate, which can be related to a system error-rate floor, if burst type errors were eliminated. If this floor is unacceptable, then another level of trouble-shooting aimed at the causes of dribbling errors is required.

Event Seconds

To aid in cause and effect diagnosis, the S5200D accumulates the number of seconds when certain parameters have occurred. Signal loss, DS3 Frame Loss, Data Sync Loss, Blue Signal detected, DS3 X-bit logic low and four TTL compatible external events are monitored. Their occurrence is recorded in separate accumulators. This provides further insight into system performance and can be useful in determining the relation between signal status, external system parameters, and error performance; particularly when the S5200D printer output is used.

Example Of Error-Second Measurement

The following shows an example of 5 error-seconds that occurred during a 12 hour overnight test. Bit measurements were made during installation prior to final system acceptance and their results are shown below.

ERROR DISTRIBUTION					
ERROR SECONDS	ERROR SECOND 1	ERROR SECOND 2	ERROR SECOND 3	ERROR SECOND 4	ERROR SECOND 5
TOTAL ERRORS	3 ERRORS	50,610 ERRORS	63 ERRORS	1 ERROR	530 ERRORS
ERROR RATE	$<1 \times 10^{-6}$	$>1 \times 10^{-3}$	$>1 \times 10^{-6}$ $<1 \times 10^{-5}$	$<1 \times 10^{-6}$	$>1 \times 10^{-5}$ $<1 \times 10^{-4}$
DRIBBLING ERRORS (ERR RATE $<10^{-6}$)	3	–	–	1	–
THRESHOLD ERROR SECONDS	–	10^{-6} thru 10^{-4}	10^{-6}	–	10^{-6} and 10^{-5}
SIGNAL STATUS EVENT SECONDS	–	FRAME LOSS AND OTHERS	–	–	–
EXTERNAL EVENTS EVENT SECONDS	–	B	A	–	A

Measurement Review

Accessing the BIT measurement TEST CATEGORY on the S5200D receiver and observing the menu of parity measurements by pushing the TEST FUNCTION button will show:

a) BIT ERR RATE=0.0E-08,TOTBIT ER=51207

The error-rate is flashing every 10^8 bits, or about 2.2 seconds indicating a current measurement. This shows the system at this time is error-free but that during the total elapsed time of the test 51,207 parity errors occurred.

b) AVG BIT ERR RATE=2.6E-08 00-12:06:51

For the 12 hours, 6 minutes and 51 seconds of testing the average error-rate was 2.6×10^{-8}. $= \frac{51207}{(43611)(44,736,000)}$

c) % BIT ERR FREE SEC=99.9885 00-12:06:51

The 5 error-seconds resulted in 99.9885% error-free seconds of tranmission. $\frac{43611-5}{43611} = 99.9885\%$

d) BIT ERR SEC= 5,TOTBIT ER= 51207

The 51,207 total errors occurred in 5 error-seconds.

e) BIT ErSecE-3=1,TOTBIT ER= 51207

f) BIT ErSecE-4= 1,TOTBIT ER= 51207

Of the 5 total error-seconds, 1 had an error that exceeded the 10^{-3} error-rate threshold, which is 4410 errors. Of course, this same error-second exceeded the 10^{-4} threshold also. Since the other 4 error-seconds had errors less than this threshold, we can determine that most of the 51,207 total errors occurred during this one second. We see from the example that this is error-second number 2.

g) BIT ErSecE-5= 2,TOTBIT ER= 51207

There were 2 error-seconds for which the error threshold exceeded 10^{-5}. Since we know one of these error-seconds exceeded 10^{-4} from the previous measurement, then one other error-second was worse than 10^{-5} but did not exceed 10^{-4}. From the example this is error-second number 5.

h) BIT ErSec-6= 3, TOTBIT ER= 51207

3 of the 5 error-seconds exceeded a 10^{-6} error threshold. Since 2 of these 3 exceeded 10^{-5} from the previous measurement, we know that 1 error-second was worse than 10^{-6} but did not exceed 10^{-5}. From the example this is error-second number 3.

i) BIT DribTOT= 2, TOTBIT ER= 51207

Total dribbling errors are the exact accumulation of the number of errors that occurred in error-seconds when the error-rate was better than 10^{-6}. Thus, of the 51,207 total errors only 4 errors were of the dribbling type. Most of the errors were of the burst type. These dribbling errors occurred in 2 error-seconds since there were 5 total error-seconds and 3 have thresholds worse than 10^{-6}. From the example these are error-seconds numbers 1 and 4.

j) BIT DribRATE=0.0E-12,TOTBIT ER= 51207

The dribbling error-rate calculation is a hypothetical error-rate based on the total dribbling errors for the elapsed time of test. The calculation is made to a limit of 0.1×10^{-12} or 10^{-13}. The dribbling error-rate of this system is actually 2×10^{-15}. Thus, if the burst error problems, which degraded the average system error-rate to 2.6×10^{-8}, were eliminated, then the system would perform well.

Error Distibution Estimates and Interpretation

From the above measurements we can make the following estimates about the system error distribution, which compared to the actual ones, are shown to be a very accurate representation of the actual error occurrences.

Error Seconds	Estimates of Errors	Actual	Err-Sec#
1	$\geq$ 44,700 but $<$51207*	50,610	2
2	$\geq$447 but $<$4470	530	5
3	$\geq$44 but $<$447	63	3
4	1 to 3	3	1
5	1 to 3	1	4

* Upper limit estimate for this error-second is more accurately the total errors less the minimum number of errors in each of the other error-seconds.

With one frame loss event-second recorded, we can estimate that it occurred during the error-second in which 44,700 to about 51,207 errors were made. This is interesting in that it gives some information about the system's DS3 framing ability. For voice systems this DS3 frame loss will cause Carrier Group Alarms (CGA's) in all connected channel banks.

The external event-seconds are shown in the example but there are not enough occurrences to make any cause and effect judgments. It is possible, however, to imagine similar results over a longer period for which the number of frame losses, 10^{-4} error-seconds, and event B occurrences were nearly equal. Other events may not show this correlation with errors. This may provide information that supports a cause and effect diagnosis. Printer error-second outputs can give more precise cause and effect correlation since each individual error-second can be observed.

Summary

Synchronous error-seconds, synchronous threshold error-seconds and event-seconds provide an extremely useful and accurate way of assessing system performance and provide a valuable maintenance and troubleshooting tool. The example has shown that with the summary measurements at the end of test provided by the S5200D receiver, a very accurate picture of the system error distribution can be obtained, and an approach to maintenance and troubleshooting can be determined.

Section 4, Operation

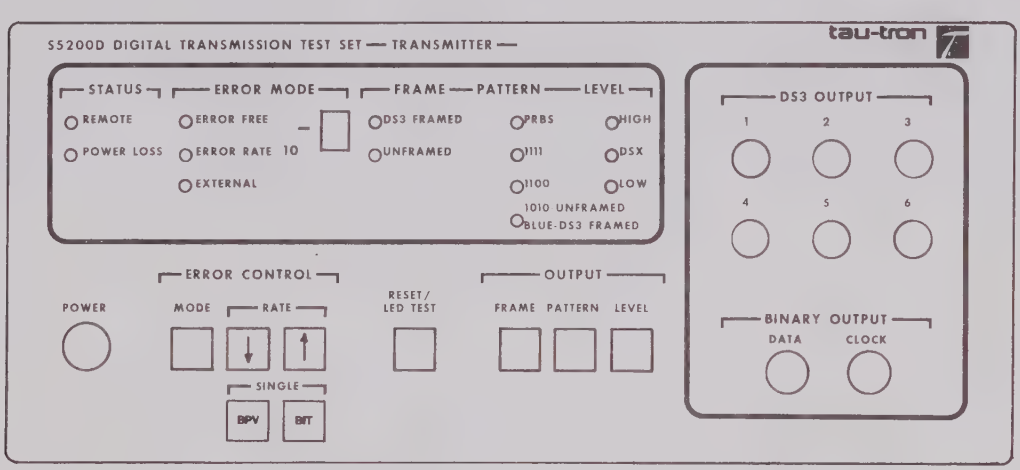
4.1 INTRODUCTION

Most S5200D transmitter functions are controllable from the front panel. Error modes, framing, pattern, and signal level functions are selected by front-panel pushbuttons. Two rear-panel switches select external error mode types (burst or rate) and short pattern types (1111, 1100, or 1010). This section provides operating procedures for all front-panel controls.

Operating procedures are presented in the order the user would most likely proceed; that is, power-on procedures are presented first, then output signal selection, error mode selection, and output connection. Each subsection contains a highlighted drawing of the front panel and step-by-step operating procedures. The front-panel drawing highlights pushbuttons and LEDs described in the subsections. Display and LED responses to pushbutton inputs are contained in the procedures.

4.1.1 **POWER-ON**

When the S5200D transmitter is installed and plugged in as described in Section 3, power may be turned on. Unlike the S5200D receiver, the transmitter does not have a specific power-on state but will power up in the same state it was in when turned off the last time. If OP-02, IEEE-488 Interface, is installed, some initial self-diagnostics are run before initialization is complete.



1. With power applied, turn on the unit by pushing the POWER button.
2. Verify that the transmitter has initialized to a valid power-up state as explained below.

   REMOTE LED should be OFF.

   POWER LOSS LED should be ON, indicating past power loss.

   One ERROR MODE LED will be ON. The Error Rate Exponent LED display will be in the range of 2 thru 9.

   One FRAME LED will be ON.

   One PATTERN LED will be ON.

   One LEVEL LED will be ON.

3. Push the RESET/LED TEST button and hold it. Verify that all LEDs come on. Release the RESET/LED TEST button and verify that the POWER LOSS LED extinguishes. All other LEDs should return to the state powered up during step 2.
4. If any problems are noted in steps 2 or 3, refer to Section 8, Service.

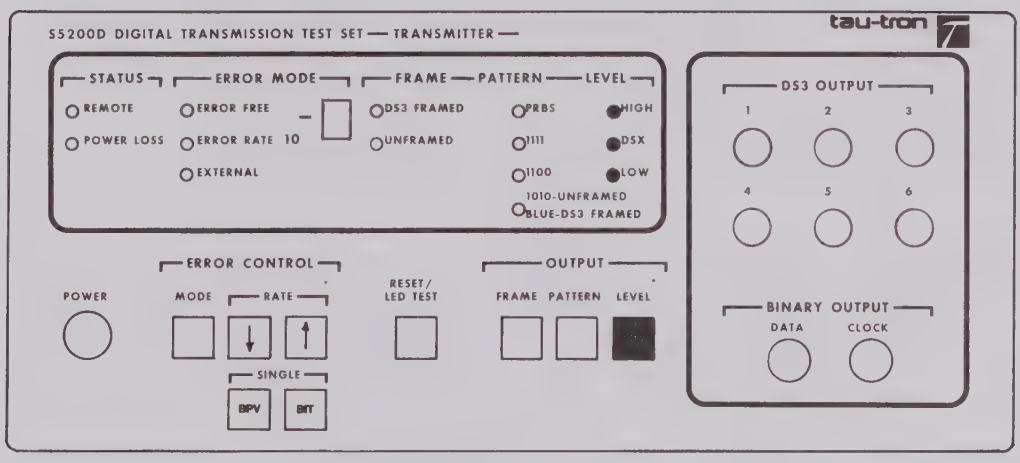
4.1.2 **POWER-FAIL RECOVERY**

Battery backup provides the S5200D transmitter with a power-fail recovery capability. When power is returned after a power failure, the S5200D transmitter lights the POWER LOSS LED and returns itself to its previous mode of operation. If the transmitter was under GPIB remote control, it returns to LOCAL control.

4.2 INPUT

4.2.1 LEVEL

The LEVEL button is used to select the desired DS3 output. This bipolar signal with B3ZS coding can be set to the HIGH, DSX and LOW levels. The binary outputs are not affected by the level button.

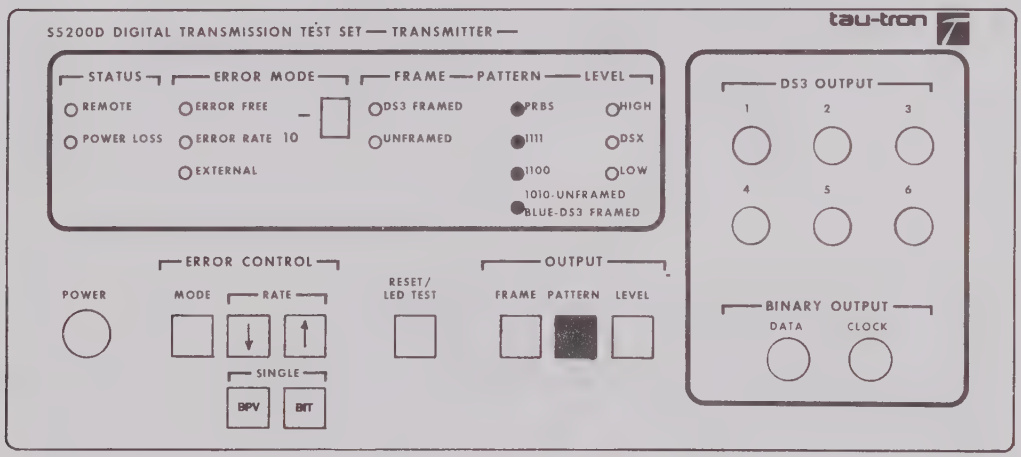


To set the DS3 output to the HIGH, DSX or LOW level;

1. Push the LEVEL button until the desired level indicated by the front-panel indicator is on.

4.2.2 **PATTERN**

The data content of the DS3 and Binary output signals can be selected by the PATTERN button. The PRBS or pseudorandom bit sequence is the Bell standard 2^{15}-1 sequence. Three short patterns can also be selected; all one's, repeating 1100 sequence and repeating 1010 sequence. These data patterns appear at the transmitter outputs in the UNFRAMED mode or are interspered with DS3 framing bits in the DS3 FRAMED mode. When in the DS3 FRAMED mode the 1010 data sequence becomes the BLUE signal, which is often used in mult-hop radio systems. In this application, a failed hop will generate the BLUE SIGNAL, transmit it down the system to inhibit downstream alarms in the DS3 transmission system. The BLUE SIGNAL should also cause all connected channel banks to go into Carrier Group Alarm.

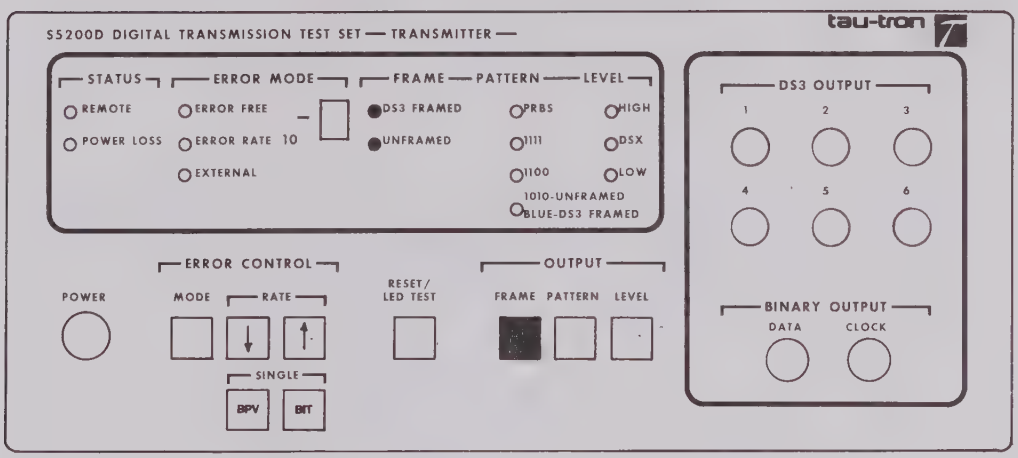


To set the data PATTERN to PRBS or the 1111, 1100, or 1010 short patterns;

1. If a SHORT PATTERN is desired, set the rear-panel SHORT PATTERN switch to the short pattern desired.
2. Push the PATTERN button until either the PRBS or the desired short pattern LED is ON.

4.2.3 **FRAME**

If the DS3 FRAMED mode is selected, the data pattern is interspersed with the DS3 housekeeping bits. One in every 85 output bits will be a DS3 housekeeping or Framing bit which include X-bits, Parity bits, M-bits, F-bits, and C-bits.



To select DS3 FRAMED or UNFRAMED;

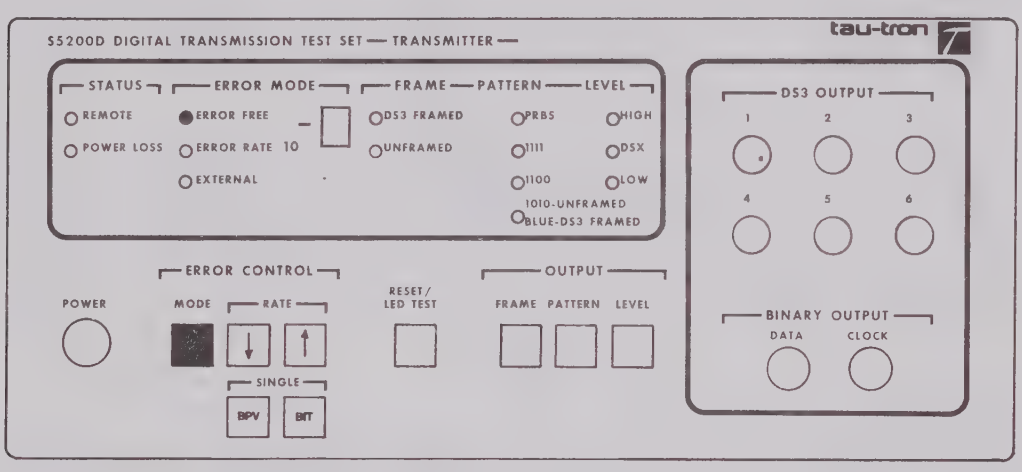
1. Push the FRAME button until the desired mode indicated by the front-panel indicator is on.

4.3 ERROR MODES

There are three modes of bit Error Insertion: ERROR FREE, ERROR RATE, and EXTERNAL. Burst or rate errors can be inserted in the EXTERNAL MODE. The ERROR MODE is controlled by the ERROR CONTROL MODE button. Single bit or BPV errors can be inserted in any error mode.

4.3.1 ERROR FREE

In the Error Free mode of operation the output data is transmitted error free.

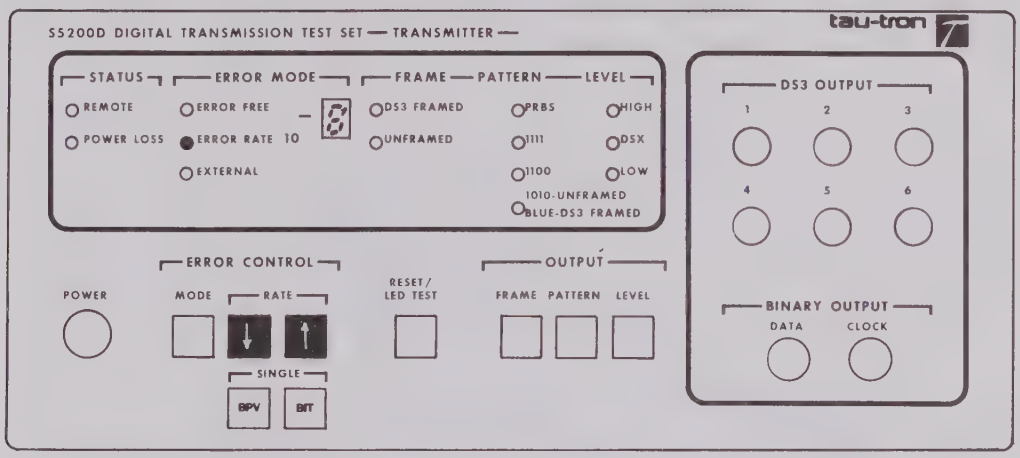


To select ERROR FREE;

1. Push the MODE button until the ERROR FREE LED on the front-panel is on.

4.3.2 INTERNAL ERROR RATE INJECTION

Eight error-rates from 10^{-9} to 10^{-2} can be inserted into the output data pattern in the FRAMED or UNFRAMED mode of operation. When in the FRAMED mode, errors are inserted in both the information bits and the DS3 Frame bits.



To select INTERNAL ERROR RATE INJECTION;

1. Set the ERROR MODE to ERROR FREE by pushing the MODE button.

NOTE The ERROR MODE SINGLE digit display will have a number from 2 to 9. This represents the bit error-rate to be inserted.

2. Set the desired error-rate by pushing the rate buttons. The down (arrow) rate button decreases the error-rate (larger number in single digit display) and the up (arrow) rate button increases the error-rate (smaller number in single digit display).

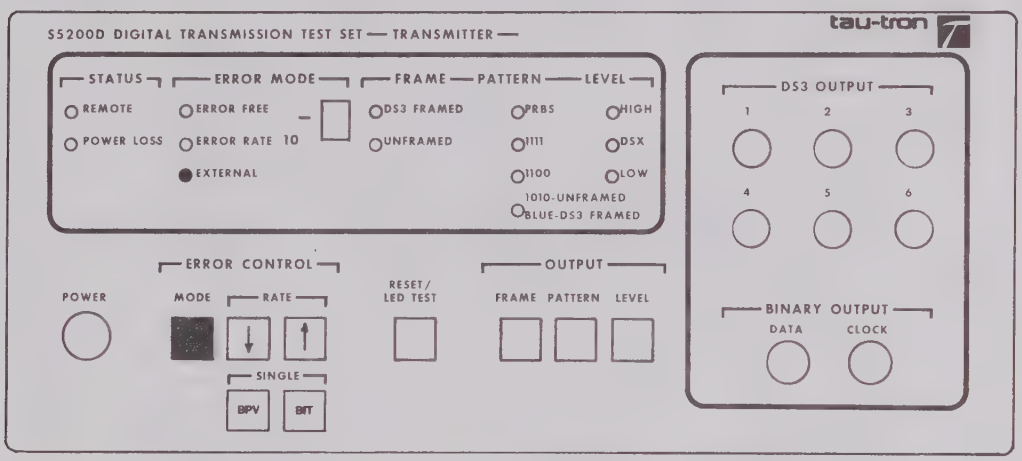
3. Push the MODE button and the error mode indicator ERROR RATE 10^{-N} will come on.

The single digit display will brighten to indicate that bit-errors are being inserted at the selected rate.

To stop internal error insertion, push the MODE button for either EXTERNAL or ERROR FREE operation.

4.3.3 EXTERNAL ERROR INJECTION

Burst errors and rate errors can be externally generated and inserted into the output data format using an external oscillator connected to the rear-panel External Error BNC. In the burst mode, the error burst rate is 100% errors during the time the oscillator input is high. In the rate mode, an error is introduced at each positive going transition at rates up to 450,000 errors per second.



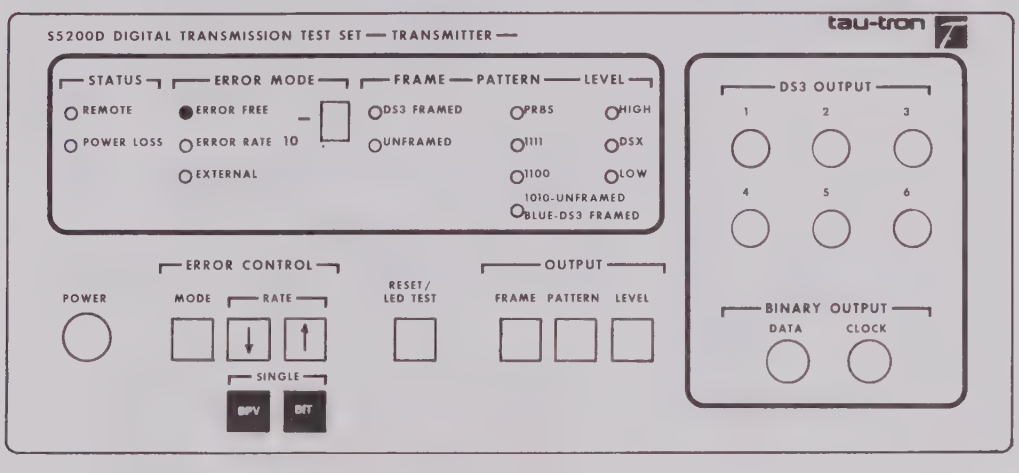
To select EXTERNAL ERROR INJECTION;

1. Push the MODE button until the EXTERNAL ERROR MODE indicator comes on.
2. Select burst or rate on the rear-panel burst rate switch.
3. Apply the external oscillator to the External Error BNC on the rear panel. The external oscillator must be capable of driving 300 ohms. The waveform must swing from less than 0.5V to greater than 3V peak.

4.3.4 SINGLE ERROR INJECTION

Single errors or Bipolar Pulse Violations (BPVs) can be inserted in the output data pattern (FRAMED or UNFRAMED) by pushing the front-panel SINGLE control buttons. When inserting either single bit errors or single BPVs, the other error type is not generated.

Single errors can be inserted in any Error Mode, but unless the initial mode is ERROR FREE, pushing the SINGLE button may overide an error being inserted, resulting in no error.



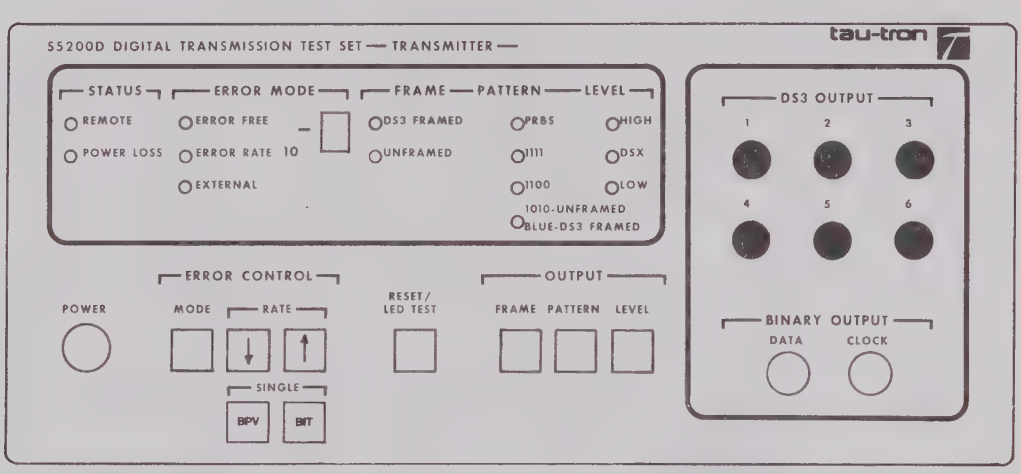
To select SINGLE ERROR INJECTION;

1. Set the transmitter to ERROR FREE by pushing the MODE button.
2. Push the SINGLE BIT for bit errors or the SINGLE BPV for single BPVs.

4.4 OUTPUT SIGNAL CONNECTIONS

4.4.1 DS3 OUTPUT

Level, data patterns and framing of the DS3 output signal can be selected by pushing the LEVEL, PATTERN, and FRAME buttons as described in the OUTPUT section. There are six DS3 outputs and they are all identical. Connection should be through a 75ohm cable to a 75ohm load. From one up to six outputs may be used simultaneously. The DS3 output connector accepts a WECo 358 connector.

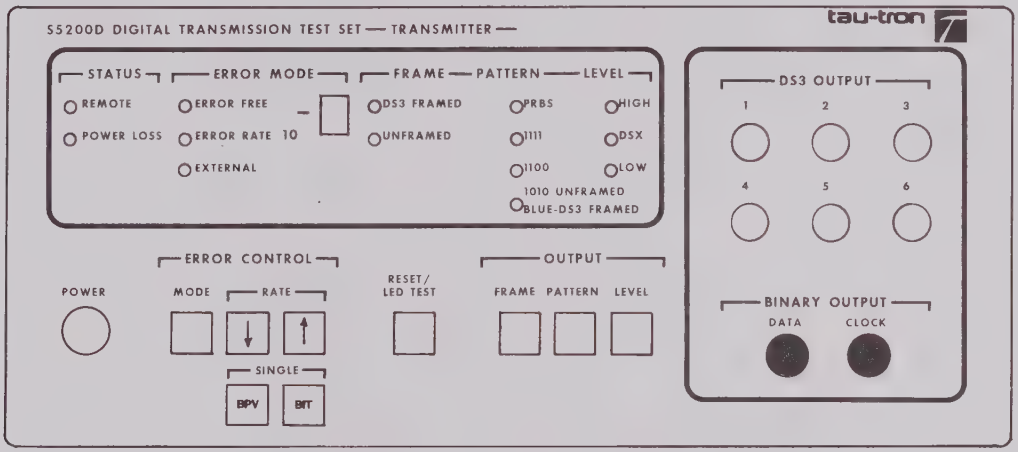


To set these connections;

1. Connect a WECo 358 connector and 75ohm cable assembly into any DS3 output.
2. Connect the other end to the DS3 equipment under test.

4.4.2 **BINARY OUTPUTS**

The BINARY DATA and CLOCK outputs have a 75ohm source impedance. Levels are ±1V peak centered around OV into a 75ohm load. Data format is non-return to zero (NRZ). The positive clock edge is in the center of the data bit. This data clock phasing can be changed 180° by having unequal data and clock cables with an 8-foot differential. When using the BINARY outputs, be sure the equipment being tested is compatible with the level and phasing characteristics of the S5200D transmitter.



To set these connections;

1. Connect the 75ohm cables with the BNC connectors to the BINARY DATA and CLOCK outputs and the equipment under test.

NOTE Cables should be of equal length for positive clock edge in the center of the data bit. In addition, equipment under test should have a 75ohm input impedance.

Section 5, Rear-Panel Interface

5.1 MONITOR CONNECTOR

A 24-pin D-Connector on the rear panel has inputs and outputs used for external monitoring. A mating connector (Tau-Tron P/N 9300-0142) is supplied with the unit.

5.1.1 SYNC OUTPUTS

There are two sync outputs, M sync and PR sync: M sync occurs once per DS3 Master Frame (4760 bits), and the PR sync occurs once per 2^{15}-1 bits of the Pseudorandom Sequence Generator.

PIN	FUNCTION	
7	M sync	Positive pulse, TTL level with 5.1kohm to +5V
18	$\overline{\text{M sync}}$	Negative pulse, TTL level with 5.1kohm to +5V
17	PR sync	Positive pulse, TTL level with 5.1kohm to +5V
5	$\overline{\text{PR sync}}$	Negative pulse, TTL level with 5.1kohm to +5V

5.1.2 POWER LOSS STATUS

A power loss status is provided on the monitor connector. Whenever the power is lost from a power failure or the front-panel ON/OFF switch is turned from off to on, the POWER LOSS status will latch until the RESET button is pushed.

PIN	FUNCTION	
10	Power Loss	Active high, TTL with 5.1kohm to +5V.
22	$\overline{\text{Power Loss}}$	Active low, TTL with 5.1kohm to +5V.

5.1.3 X-BIT INPUT

The X-Bit is a bit in the DS3 frame format that occurs once per Master Frame at about a 9.4kHz rate. This bit is normally a logic one and is recognized and counted by the S5200D receiver when it appears as a logic low. It can be set low at the rear-panel monitor connector.

PIN	FUNCTION	
21	X-Bit	TTL compatible internally held high.

5.2 BNC SIGNAL OUTPUTS

On the rear panel there are three (3) BNC connectors; EXTERNAL CLOCK IN, JITTER INJECT, and ERROR INJECT.

5.2.1 EXTERNAL CLOCK IN

The transmitter can be used with an external clock connected to the rear-panel BNC. The input impedance is 75 ohms, AC coupled and requires an 800mV minimum peak-to-peak level. When this level is reached, the transmitter will automatically switch to the external clock. In this mode of operation the range of input is 44.736MHz ± 3MHz.

5.2.2 JITTER INJECT

Not used.

5.2.3 ERROR INJECT

This input is covered in Section 4.3, Error Modes.

5.3 IEEE-488 INTERFACE (GPIB)

When option 02, IEEE-488 Interface (GPIB), is installed, the S5200D may communicate with other GPIB compatible devices as a talker/listener or listener only. This section provides an introduction to GPIB and details of S5200D transmitter operation under GPIB control.

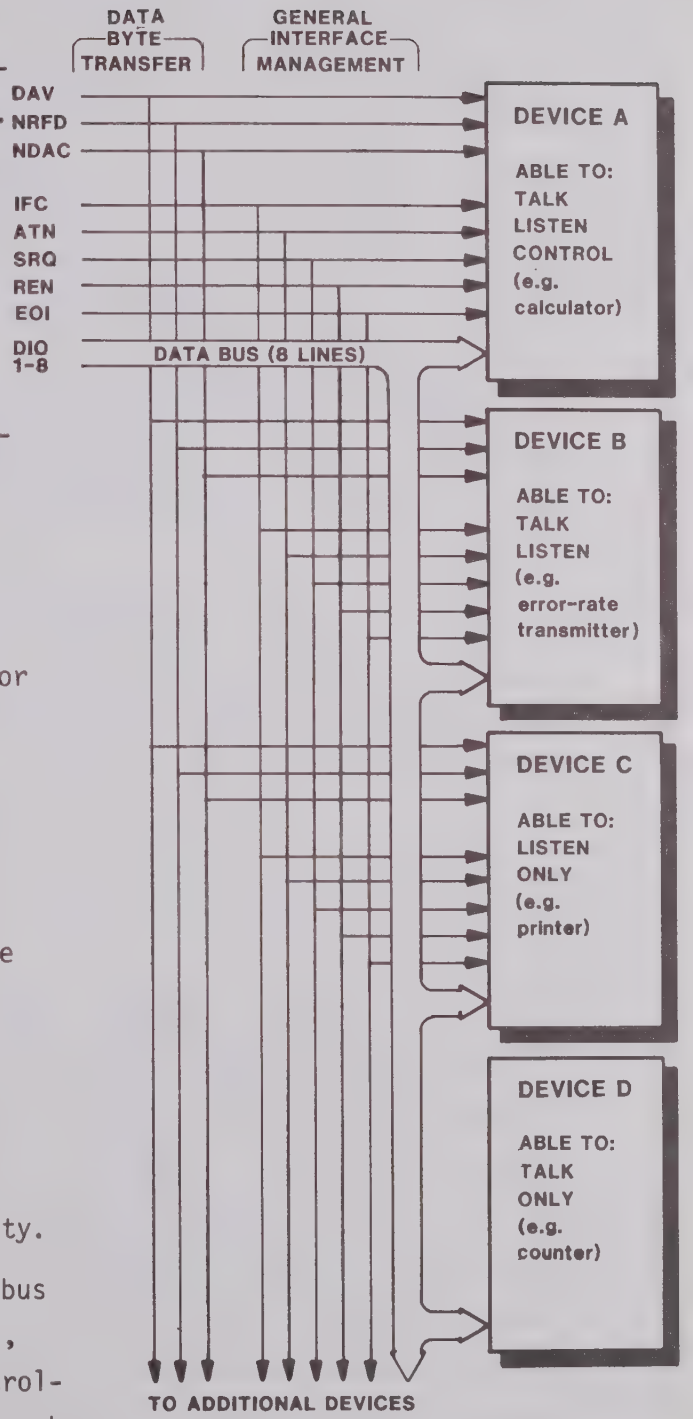
5.3.1 INTRODUCTION

Description of IEEE-488

The GPIB (General Purpose Interface Bus) transfers data and commands between the units of an instrumentation system on 16 lines. The interface functions for each unit are performed within the unit so only passive cabling is necessary to connect the system. The cables connect all instruments, controllers, and other units of the system in parallel across the signal lines.

Eight of the lines (DIO1 thru DIO8) are reserved for the transfer of data and other messages in a byte-serial, bit-parallel manner. Data and message transfer are asynchronous and are coordinated by the three handshake lines: DAV (data valid), NRFD (not ready for data), and NDAC (not data accepted). The other five lines are for control of bus activity.

Devices connected to the bus may be talkers, listeners, or controllers. The controller dictates the roll of each of the other units by setting



the ATN (attention) line true and sending talk or listen addresses on the data lines (DIO1 thru DIO8). Addresses are set into each device at the time of system configuration either by switches built into the unit or by jumpers on a printed-circuit board. While the ATN line is true, all units must listen to the data lines. When the ATN line is false, only devices that have been addressed will actively send or receive data. All others ignore the data lines.

Several listeners can be active simultaneously, but only one talker can be active at a time. Whenever a talk address is put on the data lines (while ATN is true), all other talkers should be automatically unaddressed.

Information is transmitted on the data lines under sequential control of the three handshake lines. No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as units can respond, but no faster than allowed by the slowest device being addressed as active. This permits several devices to receive the same message byte concurrently.

The ATN line is one of five control lines. When ATN is true, addresses and universal commands are transmitted on only seven of the data lines using ASCII code. When ATN is false, any code of eight bits or less understood by both the talker and listener(s) can be used.

The other control lines are IFC, REN, SRQ, and EOI. IFC (interface clear) places the interface system in a quiescent state. REN (remote enable) is used with other coded messages to select either local or remote control of each unit.

Any active unit can set the SRQ (service request) line to true. This indicates to the controller that some unit on the bus wants attention; for example, a counter on a bus may want attention because it has just completed a time-interval measurement and wants to transmit the reading to a printer.

EOI (end or identify) is used by a unit to indicate the end of a multiple-byte transfer sequence. When a controller sets both ATN and EOI lines to true, each unit capable of a parallel poll indicates its current status on the data line (DIO1 thru DIO8) assigned to it.

It is not necessary that every unit be capable of responding to all of the lines. Each unit can be designed to respond only to those lines that are pertinent to its functions on the bus.

S5200D Transmitter GPIB capabilities

The S5200D transmitter may be interfaced as a talker/listener or a listener only. No controller functions are implemented. As described in the IEEE-488-1978 (GPIB) standard, the following GPIB capabilities are implemented:

SH1 Complete source handshake.

AH1 Complete accepter handshake.

T6 Basic talker, serial poll, no talk only, unaddress if addressed to listen.

TE0 No extended talker (secondary talk address) capability.

L3 Basic listener, listen only, unaddress if addressed to talk.

LE0 No extended listener (secondary listen address) capability.

SR1 Complete service request capability.

RL2 No local lockout on remote/local capability.

PP0 No parallel poll capability.

DC1 Complete device clear capability.

DT1 Complete device trigger capability.

C0 No control capability.

E2 Tri-state drivers are used on DIO lines to achieve maximum data transfer rates.

5.3.2 GPIB INTERFACE CONNECTIONS

A 24-pin GPIB connector is provided on the rear-panel of the S5200D transmitter. Connector dimensions and pinouts correspond to IEEE specifications. The connector is mounted on all units, but is operational only on units equipped with OP-02, IEEE-488 Interface. Tri-state drivers are used on the DIO lines in the talk mode to achieve higher data-transfer rates.

5.3.3 GPIB ADDRESS AND OPTION SELECTION

When Option 02, IEEE-488 Interface (GPIB), is installed, the 8-section DIP switch on the rear panel is used for GPIB talk/listen address selection as follows:

Switch	Function (1=on=switch up)	
1(left)	SRQ Enable.....	With this switch on, the S5200D transmitter is allowed to generate service requests (assert the GPIB SRQ line). In systems with many GPIB units, this may not be desirable. Service requests can be inhibited by setting this switch down to its off position. The S5200D transmitter maintains status and will respond to serial polls regardless of the SRQ Enable setting.
2.....	Talk Only.....	This setting is ignored by the S5200D transmitter as it does not have a talk-only mode of operation.
3.....	Listen Only.....	With this switch on, the S5200D transmitter can be remotely controlled, but cannot be addressed to talk.
4.....	Address A5.....	A1 thru A5 plus two additional bits, independent of the switch settings, form a 7-bit talk and listen address. A1 thru A5 are the least-significant bits. The two additional bits are the most-significant bits and are fixed as 1-0 for a talk address, and as 0-1 for a listen address. Once the 5 address bits A1 thru A5 are selected, both talk and listen addresses are specified for the receiver.
5.....	Address A4	
6.....	Address A3	
7.....	Address A2	
8.....	Address A1	

NOTE THE DIP SWITCH IS READ ON POWER-UP ONLY. To change the S5200D transmitter's GPIB address or other characteristics, the transmitter must be turned off then back on.

5.3.4 RESPONSE TO GPIB COMMANDS

The following GPIB commands and events are responded to by the S5200D transmitter:

S5200D-TX addressed to listen
Universal unlisten commanded
S5200D-TX addressed to talk
Universal untalk commanded
Data byte received
Remote/local commanded
Device clear commanded
Device trigger commanded
Serial poll enable/disable commanded

Several GPIB capabilities are not supported by the S5200D transmitter. The following commands are ignored by the transmitter:

Local lockout
Identify (parallel poll trigger)
Secondary addresses
Parallel poll configure/unconfigure
Parallel poll enable/disable
Take control

The following paragraphs detail the GPIB commands and events to which the S5200D transmitter will respond.

5.3.4.1 S5200D TRANSMITTER ADDRESSED TO LISTEN

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1								INTERFACE MANAGEMENT ATN EOI SRQ IFC REN				
MLA	Y	O	1	L5	L4	L3	L2	L1	1	X	X	X	X

L1-L5 specify the device dependent bits of the device's listen address as set by the rear-panel DIP switch.

When MLA my listen address is present on the GPIB bus, the S5200D transmitter will be addressed to listen. If previously addressed to talk, the transmitter will automatically untalk. The transmitter cannot be configured to talk and listen at the same time in order to prevent its talk data from being interpreted as commands.

5.3.4.2 UNIVERSAL UNLISTEN COMMANDED

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
UNL	Y O 1 1 1 1 1 1	1 X X X X

When UNL unlisten is present on the GPIB bus, the S5200D transmitter will cease to listen and addressed commands (GET, GTL, and SDC) and data will be ignored. Universal commands (IFC, REN, DCL, SPE, SPD, MLA, and MTA) will continue to be recognized and responded to.

5.3.4.3 S5200D TRANSMITTER ADDRESSED TO TALK

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
MTA	Y 1 O T5 T4 T3 T2 T1	1 X X X X

T1-T5 on the DIO lines specify the device dependent bits of the device's talk address as set by the rear-panel DIP switch.

When MTA my talk address is present on the GPIB bus, the S5200D transmitter will be addressed to talk. If previously addressed to listen, the transmitter will automatically unlisten to prevent output data from being interpreted as commands. Since a GPIB system can have only one talker, unique talk addresses must be selected for each device in the system. All other devices must untalk when the transmitter is addressed to talk. If addressed to talk after SPE (serial poll enable) and before SPD (serial poll disable), the transmitter will respond by putting its status byte on the DIO lines (described later under Service Request and Serial Poll). Otherwise, transmitter output data (i.e., status) will be placed on the DIO lines. If the transmitter has nothing to say, it will output one or two null bytes along with EOI.

5.3.4.4 UNTALK COMMANDED

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
UNT	Y 1 O 1 1 1 1 1	1 X X X X
OTA	OTA = SGA ∧ $\overline{\text{MTA}}$	

The UNT code is provided for system use.

The presence of UNT untalk command or a talk address other than the S5200D transmitter's (OTA other talk address) causes the transmitter to become unaddressed to talk. If service requests are not inhibited and the transmitter still has data it wishes to output, a service request indicating request-to-talk will be generated.

5.3.4.5 DATA BYTE RECEIVED

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
ATN	X X X X X X X X	1 X X X X
DAB	D D D D D D D D 8 7 6 5 4 3 2 1	0 X X X X

D1-D8 specify the device dependent data bits. The source of the message on the ATN line is always the C function, whereas the messages on the DIO and EIO lines are enabled by the T function.

When the GPIB ATN attention line is inactive and the S5200D transmitter is addressed to listen, bytes received on the eight DIO lines will be interpreted as device-dependent commands (see 5.3.5, Device-Dependent Commands).

5.3.4.6 INTERFACE CLEAR COMMANDED

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
IFC	X X X X X X X X	X X X 1 X

When the IFC interface clear line is asserted on the GPIB bus, the S5200D transmitter reinitializes its interface functions as described by IEEE-488-1978 state diagrams. A pending service request will be cleared. The stauts byte in the transmitter is not cleared, however. It may be polled to determine if bus errors, indicated in the status byte, may have caused bus problems prior to the interface clear command. If in remote mode, reception of the interface clear command does not return the S5200D-TX to local.

5.3.4.7 REMOTE/LOCAL COMMANDED

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
GTL	Y O O O O O O 1	1 X X X X
LLO	Y O O 1 O O O 1	1 X X X X
REN	X X X X X X X X	X X X X 1

When the REN remote enable line is asserted on the bus and the S5200D transmitter is addressed to listen, the transmitter is put in remote mode. Since the transmitter has no return-to-local front-panel control, local lockout capability is not provided. While in remote mode, all local control (front-panel pushbuttons) is disabled. The transmitter may be remote-enabled only by first asserting the REN line under remote control. REN going inactive will return it to local control. If addressed to listen and in remote, the presence of the GTL go to local message returns the transmitter to local control. LLO local lockout is ignored at all times.

The transmitter responds to commands issued by GPIB only when it is in remote mode. Commands issued while the transmitter is under local control are saved. When the S5200D-TX is put into remote mode, previously issued GPIB commands take effect.

When the transmitter is returned to local control, it returns to the mode previously selected by front-panel control. If any buttons were pushed while the transmitter was under remote control, the transmitter's mode reflects those button selects when returned to local.

5.3.4.8 DEVICE CLEAR COMMANDED

CODE	DATA BUS DIO 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
DCL	Y O O 1 O 1 O O	1 X X X X
SDC	Y O O O O 1 O O	1 X X X X

When under remote control, the S5200D transmitter may be cleared by DCL universal device clear or SDC selective divice clear. SDC is accepted only if the S5200D is currently addressed to listen. DCL is responded to whether addressed to listen

or not, as long as the transmitter is under remote control. In response to a device clear command, the transmitter functions are returned to the following states:

```
ERROR MODE           = ERROR FREE
ERROR RATE EXPONENT  = 9
FRAME MODE           = FRAMED
PATTERN              = PRBS
LEVEL                = DSX
```

The transmitter will remain under remote control, and the power loss history status will be cleared. The transmitter's GPIB interface is not reinitialized. When the transmitter is in local mode, device clear causes the software to return to the status listed above. The transmitter will not return to those states until it is put in remote mode.

5.3.4.9 DEVICE TRIGGER COMMANDED

CODE	DATA 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
GET	Y O O O 1 O O O	1 X X X X

The S5200D transmitter takes no action in response to GET group execute trigger being present on the bus.

5.3.4.10 SERIAL POLL ENABLE/DISABLE COMMANDED

CODE	DATA 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
SPD	Y O O 1 1 O O 1	1 X X X X
SPE	Y O O 1 1 O O O	1 X X X X

The SPE serial poll enable and SPD serial poll disable commands are recognized by the S5200D transmitter when they are present on the bus. In response to a serial poll, the transmitter will put its GPIB status byte on the DIO lines. The serial poll command sequence and status byte interpretation are described later under Service Request and Serial Poll.

5.3.4.11 UNSUPPORTED GPIB COMMANDS

CODE	DATA 8 7 6 5 4 3 2 1	INTERFACE MANAGEMENT ATN EOI SRQ IFC REN
IDY	X X X X X X X X	1 1 X X X
LLO	Y O O 1 O O O 1	1 X X X X
MSA	Y 1 1 S5 S4 S3 S2 S1	1 X X X X
OSA	OSA = SCA ∧ $\overline{\text{MSA}}$	
PPC	Y O O O O 1 O 1	1 X X X X
PPE	Y 1 1 O S P3 P2 P1	1 X X X X
PPD	Y 1 1 1 D4 D3 D2 D1	1 X X X X
PPU	Y O O 1 O 1 O 1	1 X X X X
TCT	Y O O O 1 O O 1	1 X X X X

S1-S5 specify the device dependent bits of the device's secondary address. S specifies the sense of the PPR, for S=O, response=O, for S=1, response=1. P1-P3 specify the PPR message to be sent when a parrallel poll is executed. D1-D4 specify don't - care bits that shall not be decoded by the receiving device . It is recommended that all zeros be sent.

No parallel poll functions (IDY identify, PPC parallel poll, PPE parallel poll enable, PPD parallel poll disable, and PPU parallel poll unconfigure), LLO local lockout, or control functions (TCT take control) are supported by the S5200D transmitter. The occurrence of these commands on the bus is ignored at all times. Undefined GPIB commands received with the ATN line asserted are also ignored.

5.3.5 DEVICE-DEPENDENT COMMANDS

All S5200D transmitter capabilities controllable from the front panel may be remotely controlled. A set of device-dependent commands issued on the GPIB bus selects the S5200D-TX commands. When the S5200D-TX is addressed to listen, data accepted on the DIO lines is interpreted as transmitter commands.

Programming the transmitter in remote control is as simple as programming it by front-panel entry. Nine commands correspond to the front-panel pushbuttons. Five additional commands are provided to return transmitter status to the controller. The table on the opposite page summarizes the device-dependent commands.

5.3.5.1 COMMAND SEQUENCE FORMATS

All device-dependent command sequences must be issued in the following format:

CMD1 (delimiter, CMD2) (delimiter, CMD3) ... CR LF

CMD1, 2, 3, etc. are any of the mnemonics shown in the table on the following page. Each character of the command sequence is read as a 7-bit ASCII code off the DIO lines. Multiple commands in a command sequence must be delimited by any of the following valid delimiters. Every command sequence must be terminated by a carriage return and line feed.

Delimiter		ASCII Code (hex)
SP	(blank).....	20
NULL	(null byte).....	00
,	(comma).....	2C
;	(semicolon).....	3B
HT	(tab).....	09

5.3.5.2 COMMAND ERRORS

Invalid commands are ignored by the transmitter. If a multiple command sequence contains an invalid command, valid commands in the sequence will still be interpreted and responded to. Invalid mnemonics cause the command error bit to be set in the transmitter's serial poll status word. If service requests are enabled, command errors also generate a service request.

DEVICE-DEPENDENT COMMANDS

REMOTE COMMAND	CORRESPONDING KEY	FUNCTION
MD	MODE	Select error-free, error-rate inject, or external error inject.
DN	↓	Decrease error-rate (NOTE: error-rate of 10^{-3} is decrease from 10^{-2})
UP	↑	Increase error-rate
BP	BPV	Inject single BPV error
BI	BIT	Inject single BIT error
RS	RESET/LED TEST	Reset power loss LED; does not perform LED test.
FR	FRAME	Select framed/unframed transmit mode
PA	PATTERN	Select PRBS, 1111, 1100, or 1010 pattern
LV	LEVEL	Select high/DSX/low signal level
MD?	none	Snapshot transmitter mode
RT?	none	Snapshot current error injection rate
FR?	none	Snapshot current frame mode
PA?	none	Snapshot current pattern
LV?	none	Snapshot current transmit level.

5.3.6 S5200D TRANSMITTER OUTPUT TO GPIB

Five output commands allow transmitter status to be snapshot and queued for output to the bus. The format and function of these five commands are shown in the table and described below. The output commands may be issued individually or in a sequence as described.

In response to the MD? command, the transmitter error mode and remote/local status will be snapshot and a corresponding ASCII mnemonic queued for output to the bus. The error modes and corresponding mnemonics are as follows:

MODE	MNEMONIC
local, error free	LOCFRE
local, error rate insert	LOCINS
local, external error	LOCEXT
remote, error free	REMFRE
remote, error rate insert	REMINS
remote, external error	REMEXT

In response to the RT? command, the transmitter error insertion rate will be snapshot and queued for output to the bus. Error-rates and the output ASCII mnemonics are as follows:

ERROR RATE	MNEMONIC
10^{-9}	E-9
10^{-8}	E-8
10^{-7}	E-7
10^{-6}	E-6
10^{-5}	E-5
10^{-4}	E-4
10^{-3}	E-3
10^{-2}	E-2

In response to the FR? command, the transmitter snapshots its current framing mode and queues it for output to the bus. When framed, the three-letter ASCII mnemonic FRM is output. When unframed, UNF is output.

In response to the PA? command, the transmitter pattern is snapshot and queued for output. Patterns and their corresponding four-character ASCII mnemonics are as follows:

PATTERN	MNEMONIC
pseudorandom bit sequence	PRBS
fixed 1111	1111
fixed 1100	1100
fixed 1010 (blue signal)	1010

In response to the LV? command, the transmitter snapshots and queues for output its current transmit level. DSX, LOW, and ØHI are the ASCII mnemonics associated with DSX cross-connect, LOW, and HI level outputs. (Ø is an ASCII space character).

Each output mnemonic is followed by an ASCII carriage return and line feed (CR and LF). If the command sequence MD?, RT?, FR? is issued and the transmitter is currently set up for local control, error-free, 10^{-9} error-rate, framed, the ASCII message queued for output would be LOCFRE CR LF E-9 CR LF FRM CR LF. When the S5200D transmitter is addressed to talk, queued data are output on the bus. When the transmitter has no more data queued for output, it will place one or two null bytes on the DIO lines along with the EOI signal.

5.3.7 SERVICE REQUEST AND SERIAL POLL RESPONSE

Several conditions detected in the S5200D transmitter will cause it to request service of the GPIB controller. The ability of the transmitter to request service may be inhibited by the rear-panel DIP switch as described in Section 5.3.3., GPIB address and option selection.

When the controller detects a service request, it should serial poll the transmitter to determine if the transmitter is requesting service and why. In response to a serial poll addressed to the S5200D transmitter, the transmitter will place its 8-bit GPIB status byte on the DIO lines. The transmitter clears its status byte when it receives a serial poll disable (SPD) command. The GPIB status byte is also cleared on power-up and in response to device clear. Only the service request bit in the status byte is reset by an interface clear.

5.3.7.1 SERVICE REQUEST, GPIB STATUS BYTE

	MOST-SIGNIFICANT HEX DIGIT				LEAST-SIGNIFICANT HEX DIGIT			
	7	6	5	4	3	2	1	0
GPIB Status Byte	0 (unused)	RQS	0 (unused)	Power Loss	Instr fail	Cmd error	Bus error	Talk request

The following transmitter-detected conditions will cause it to request service (if SRQ is enabled):

Bus error.....Bus error occurs when the transmitter is addressed to talk with no listeners active on the bus. Since a source handshake may have been started by the talking receiver with no acceptor to complete the handshake, this error may hang up the bus. This condition can be cleared and detected by the controller issuing an interface clear followed by a serial poll. The ON condition for the bit is 1.

Cmd error.....Command error occurs when the transmitter detects an invalid device-dependent command as described earlier under Device-Dependent Commands. The command error bit is set in the GPIB status byte. The ON condition for the bit is 1.

Talk request.....When the S5200D transmitter has data to output, but has not been configured to talk, it will generate a service request with the talk request bit set in the GPIB status byte. The ON condition for the bit is 1. If configured to talk before serial polled, this bit will be cleared in the status byte. If no other bits are set, the service request will be deasserted.

Inst fail.....A software detected failure in the S5200D transmitter will cause the instrument failure bit to be set in the GPIB status byte. Some instrument failures may not be recoverable by device clear functions. The only recourse, then, is to turn the receiver off and back on. The ON condition for the bit is 1.

Power Loss.....When a power loss is detected, the power loss bit is set in the GPIB status byte. When power is restored, this bit will remain set until either the device clear or RESET (RS) command is issued or the transmitter is serial polled. The ON condition for the bit is 1.

The RQS bit is ON (1) whenever one or more of the other bits (power loss, instrfail cmd error, bus error, or talk request) is ON and service requests have been enabled by DIP switch 1.

Multiple bits may be set in the status byte when it is polled. All bits are cleared following a serial poll.

Status displayed by front-panel LEDs is not available through the GPIB status byte acquired by serial polling. The transmitter status may be obtained as described earlier under S5200D-TX output to GPIB.

The S5200D transmitter will not respond to parallel polling commands.

5.3.7.2 SERIAL POLLING

The GPIB status byte may be accessed from the S5200D transmitter by serial polling as follows:

1. Issue 'UNT' universal untalk command.
2. Issue 'SPE' serial poll enable command.
3. Issue controller listen address.
4. Issue 'MTA' S5200D transmitter talk address.
5. Receive 'STB' S5200D transmitter status byte.

6. Issue 'UNT' or 'OTA' S5200D transmitter untalk command.
7. Issue 'SPD' serial poll disable command.

NOTE A random loss of the RQS bit may occur after the transmitter has generated a service request and has been polled. It is recommended that the user check for any bits set in the serial poll status word to determine if the transmitter may have requested service.

5.3.8 SAMPLE GPIB CONTROL

All S5200D functions controllable from the front panel may be remotely controlled using GPIB. In addition, transmitter status conveyed locally by front-panel LEDs and a seven-segment display may be accessed under remote control. This section provides samples of GPIB control and status acquisition.

5.3.8.1 TRANSMITTER MODE CONTROL

If the user is familiar with the S5200D transmitter and has operated the instrument manually, then controlling it by GPIB is very simple. Remote control commands exactly imitate front-panel pushbuttons. Consider the following example. Assume the transmitter is initially set up to generate an error-free, DS3 framed, pseudo-random bit pattern at the DSX signal level. To manually select the same signal level and format at an error insertion rate of 10^{-7}, the user pushes the up (arrow) RATE button twice to increase the error-rate from 10^{-9} to 10^{-7} then pushes the MODE button once to change from error-free to error-rate insertion. Under remote control, the user would simply issue the command sequence UP, UP, MD CR LF to accomplish the same setup change. Device-dependent commands are received by the transmitter only when it is addressed to listen. The controller must place the transmitter's listen address on the parallel data lines (DIO1-DIO8) with the ATN (attention) line asserted to configure the transmitter to listen. Device-dependent commands are accepted and processed whether the transmitter is under local or remote control. However, remote commands take effect only when the transmitter is under remote control. When the REN (remote enable) line is asserted and the transmitter is addressed to listen, its REMOTE LED will light and previously issued remote commands will take effect. When the transmitter, is addressed to listen with the ATN not asserted, data placed on the bus is accepted as device-dependent commands (see Section 5.3.5, Device-Dependent commands).

The following example illustrates how GPIB can be used to select an unframed PRBS transmitter HIGH signal with 10^{-4} error insertion rate:

1. With power OFF, set rear-panel DIP switches as follows to enable service requests and select talk address = 41 (hex), listen address = 21 (hex):

SWITCH:	1	2	3	4	5	6	7	8
SETTING:	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON

2. Turn power on.

3. Assert REN line.

4. Issue DCL (device clear) to put transmitter in known state (error-free, 10^{-9}, framed, PRBS, DSX). Since the transmitter is still in local control, the new state will not take effect until the transmitter is addressed to listen with REN asserted.

5. Assert ATN line and issue listen address. Transmitter REMOTE LED will light and transmitter will go to known state.

6. Issue UP, UP, UP, UP, UP, MD CR LF to select 10^{-4} error-rate insertion. This sequence is identical to pushing the up arrow button five times followed by the MODE button.

7. Issue FR, LV, LV CR LF to select unframed high level signal. This sequence is identical to pushing the FRAME button once, followed by the LEVEL button twice.

Note that command sequences are output one character at a time and must be terminated by a carriage return and line feed.

5.3.8.2 GETTING STATUS FROM THE S5200D TRANSMITTER

After issuing a command sequence such as the one described above, a controller may wish to verify the transmitter has been properly set up. The five query commands (MD?, RT?, FR?, PA?, and LV?) snapshot transmitter status and queue it for output to the bus. When the transmitter is addressed to listen, the ASCII-encoded status message will be placed on the DIO lines. Assuming the transmitter has been set up as described in Section 5.3.8.1, transmitter status may be accessed as follows:

1. Assert ATN line and issue transmitter listen address. Transmitter REMOTE LED will remain on.
2. Issue MD?, RT?, FR?, PA?, LV? CR LF command sequence to query transmitter mode, error-rate, framing, pattern, and level.
3. Issue universal unlisten command.
4. Configure controller to listen.
5. Assert ATN and issue transmitter talk address.
6. Receive five status mnemonics from transmitter, separated by carriage return and line fad. If transmitter was set up as described in Section 5.3.8.1, the following ASCII status messages would be returned:

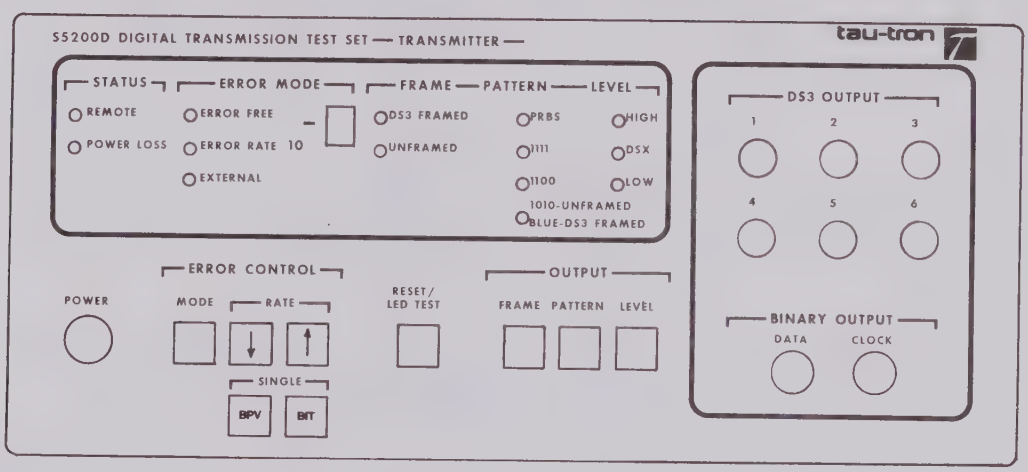
   REMINS CR LF E-4 CR LF UNF CR LF PRBS CR LF HI CR LF

Section 6, Performance Verification

6.1 TRANSMITTER PERFORMANCE VERIFICATION

These tests can be made with the S5200D transmitter alone to provide a partial check on its operation. They also provide an introduction to the operation and capabilities of the unit.

More thorough checks, particularly of the output circuits, require an S5200D receiver. These checks are included in the next section "Transmitter Verification with Receiver".



6.1.1 TRANSMITTER POWER-UP

1. Turn on transmitter POWER. Yellow POWER LOSS STATUS indicator will light.

   Push and hold RESET/LED TEST. All STATUS, ERROR MODE, FRAME, PATTERN, and LEVEL indicators will light.

   Release RESET/LED TEST. Yellow POWER LOSS STATUS indicator will extinguish (no STATUS indicator will be lit) and only one ERROR MODE, FRAME, PATTERN, and LEVEL indicator will be lit.

   If this condition is not obtained, refer to Section 8, service.

6.1.2 ERROR MODE AND CONTROL

1. Repetitively push the ERROR CONTROL MODE button. ERROR MODE indicators (ERROR FREE, ERROR RATE, and EXTERNAL) will light one at a time. Leave at point where yellow ERROR RATE 10^{-N} is lit (N is numeric indicator which brightens in ERROR RATE mode).

2. Repetitively push the down (arrow) button. ERROR RATE numeric exponent indicator number will increase by one for each push up to 9. Repetitively push the up (arrow) button. ERROR RATE numeric exponent indicator will decrease by one for each push down to 2. Set at 5 and set MODE to ERROR FREE.

6.1.3 FRAME

1. Repetitively push the OUTPUT FRAME button. FRAME indicators (DS3 FRAMED and UNFRAMED) should light one at a time. Leave at DS3 FRAMED.

6.1.4. PATTERN

1. Set rear-panel Short Pattern switch up to 1111 and repetitively push the OUTPUT PATTERN button. PATTERN indicators (PRBS and 1111) will light one at a time.

2. Set rear-panel Short Pattern switch to the center 1100 position and repetitively push the OUTPUT PATTERN button. PATTERN indicator (PRBS and 1100) will light one at a time.

3. Set rear-panel Short Pattern switch down to 1010 and repetitively push the OUTPUT PATTERN button. PATTERN indicators (PRBS and 1010) will light one at a time. Leave the rear-panel Short Pattern switch down at 1010 and the PATTERN at PRBS.

4. Repetitively push the OUTPUT LEVEL button. LEVEL indicators (HIGH, DSX, and LOW) will light one at a time. Leave at DSX.

6.1.5 **POWER LOSS RECOVERY**

1. Turn POWER off then back on. The following indicators will light (indicating last control settings have been remembered):

   STATUS.....POWER LOSS
   ERROR MODE....ERROR FREE
   FRAME.....DS3
   PATTERN.....PRBS
   LEVEL.....DSX

2. Push RESET/LED TEST to extinguish POWER LOSS indicator.

6.2 TRANSMITTER VERIFICATION WITH RECEIVER

These tests must be made with an S5200D receiver and, together with the Transmitter Performance Verification test of the previous section, provide a comprehensive check of the transmitter operation.

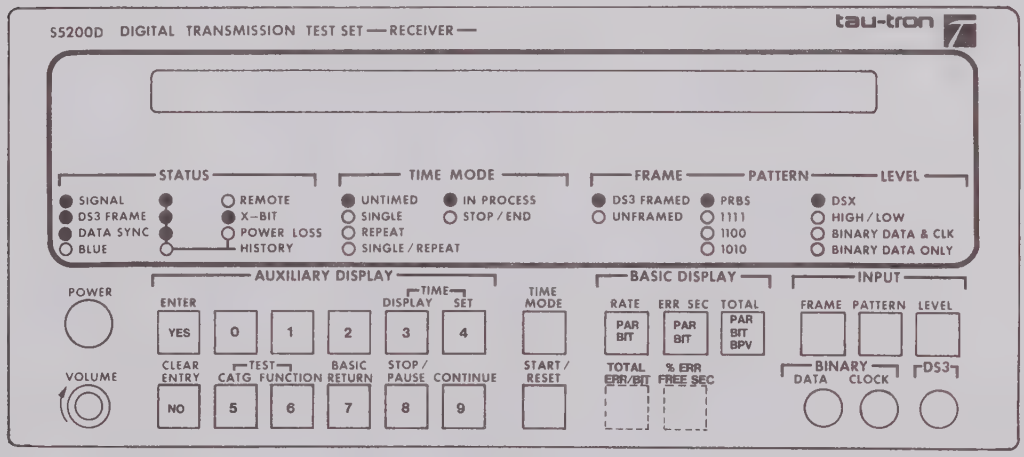
It is required that the checks of the Transmitter Performance Verification section be done before the checks of this section.

These checks will verify operation of functions performed by all elements of the S5200D transmitter.

The verification checks are:

Output Level, B3ZS
Pattern
Frame
Error Inject
Output Binary

6.2.1 RECEIVER SETTINGS



1. Turn the Receiver POWER on. Verify "power-up" state of LEDs as shown above. Display will read.

   PAR ERR RATE = xx TOTPAR ER = xx

NOTE When the alphanumeric display numerals are given as "xx", the actual values shown are not important.

If this condition is not obtained, refer to the Receiver Service Section.

6.2.2 DSX-LEVEL, PRBS PATTERN, DS3 FRAME

1. Turn the transmitter POWER on.

2. Set the following conditions:

   Front panel:

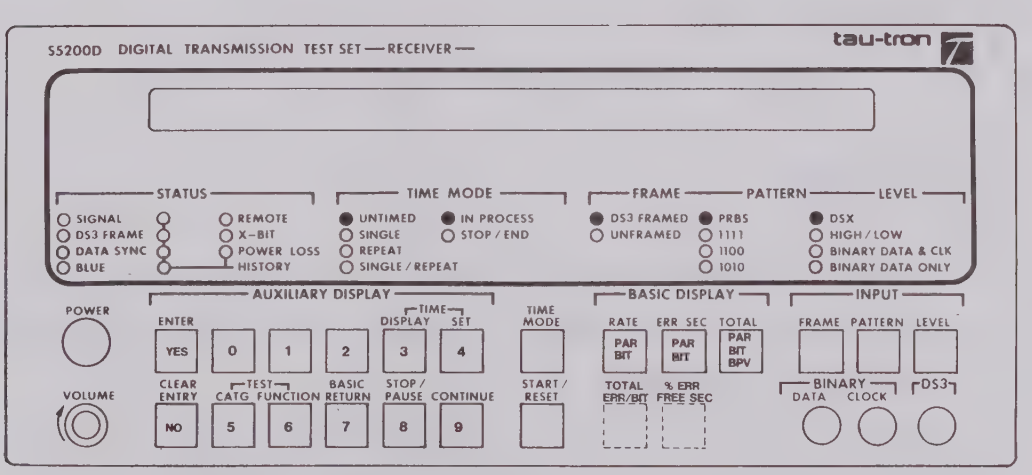
   LEVEL.....DSX
   PATTERN.....PRBS
   FRAME.....DS3 FRAMED
   ERROR MODE.....ERROR FREE

   Rear panel:

   SHORT PATTERN.....1010

3. Connect the transmitter to the receiver using a 75ohm (RG59/U) cable with WECo type 358 connections (Trompeter P/N PCW-XX-75 or equivalent).

4. Push receiver START/RESET. Observe the LED'S:



5. Observe the display:

   PAR ERR RATE = 0.0E-08 TOTPAR ER = 0

   This verifies transmitter LEVEL-DSX, PATTERN - PRBS, and FRAME- DS3-FRAMED.

   If this condition is not obtained and the receiver has passed all checks, then the trouble is in the transmitter. Check the Service Section for the transmitter.

6.2.3 HI/LOW LEVEL, BLUE-PATTERN, UNFRAMED

1. Set the transmitter OUTPUT LEVEL to LOW. Set the receiver INPUT LEVEL to HIGH/LOW and push the receiver START/RESET button. Observe the receiver display:

   PAR ERR RATE = 0.0E-08 TOTPAR ER = 0

2. Set the transmitter OUTPUT LEVEL to HIGH. Push the receiver START/RESET button and observe the receiver display:

   PAR ERR RATE = 0.0E-08 TOTPAR ER = 0

3. Set the transmitter PATTERN to BLUE-DS3 FRAMED. Observe the receiver status DATA SYNC (red and yellow LEDs) on and BLUE (yellow LED) on.

4. Set the transmitter FRAME to UNFRAMED. Observe the receiver status DS3 FRAME (red and yellow LEDs) on.

6.2.4 ERROR INJECTION

1. Restore the transmitter front-panel settings to:

   LEVEL-DSX
   PATTERN-PRBS
   FRAME-DS3 FRAMED
   ERROR MODE-ERROR FREE

2. Set the ERROR MODE to ERROR RATE 10^{-5}. Set the receiver LEVEL TO DSX. Push the receiver START/RESET button and observe the receiver LED condition as in step 4 and observe the display:

   PAR ERR RATE = 1.0E-05 TOTPAR ER = xx

   The parity error-rate will update every 2.2 seconds (approx.).

3. Set the transmitter ERROR MODE to ERROR FREE. Push the receiver START/RESET button and push the transmitter SINGLE BPV and BIT once each. Push the receiver BASIC DISPLAY-TOTAL button once and observe the display:

   TOTBIT ER = 1

   Push again and observe the display. TOTBPV ER = 1

6.2.5 **BINARY OUTPUTS**

1. Disconnect the 75ohm coaxial cable. Connect the BNC cables between the following:

Transmitter	Receiver
Binary output data	Binary data
Binary output clock	Binary clock

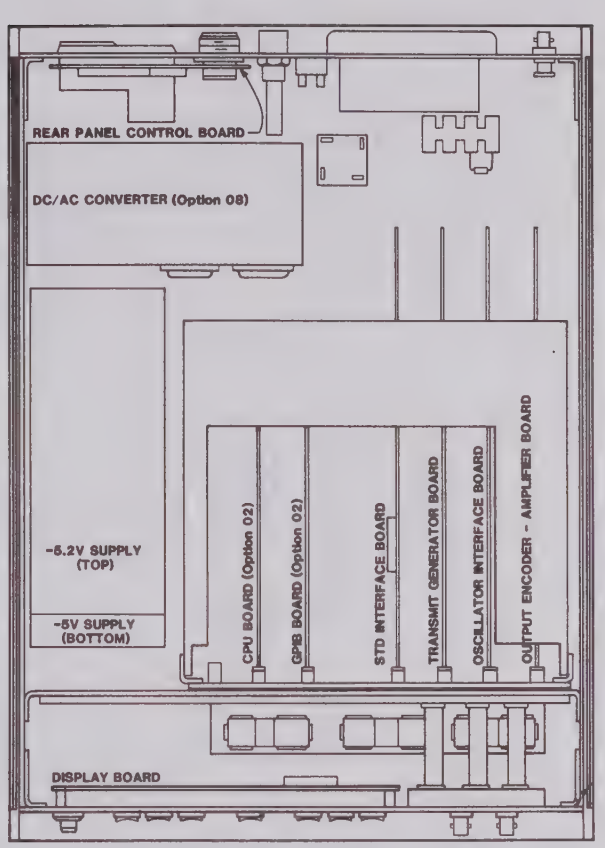
2. Set the receiver LEVEL to BINARY DATA AND CLOCK. Push the receiver START/RESET and observe the receiver display:

PAR ERR RATE = 0.0E-08 TOTPAR ER = 0

Section 7, Theory of Operation

7.1 GENERAL

The S5200D transmitter consists of four plug-in printed circuit boards, a front-panel display board, and a rear-panel printed circuit board (refer to block diagram). If Option 02, IEEE-488 Interface, is installed, two additional plug-in circuit boards are installed. Two power supplies are used, a +5V supply at 12A and a -5.2V supply at 6A. An optional DC power converter allows operation from either -24VDC or -48VDC , or 115VAC.



The six plug-in boards are divided into two sections:

High-Speed section:

- Oscillator Interface board
- Transmit Generator board
- Output Encoder-Amplifier board

Software/Hardware section:

- CPU board (OP-02 only)
- GPIB board (OP-02 only)
- STD Interface board

All four (or six) plug-in boards plug into a mother board which is also divided into the same two sections, high-speed and software/hardware. The software/hardware section uses a STD 8-bit microprocessor system bus.

REMOTE CONTROL

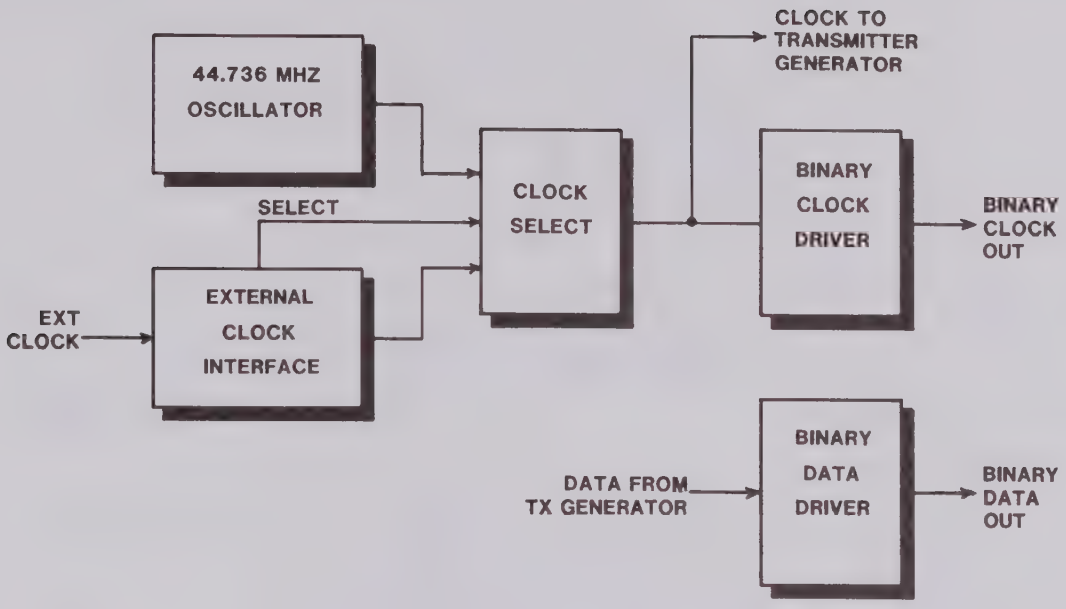
When Option 02, IEEE-488 Interface, (GPIB), is installed, two printed circuit boards are added and a third one is built-up to full capability:

CPU board.....Added

GPIB board.....Added

STD Interface board.....Built-up to provide a switching capability between local front-panel control and remote GPIB control.

7.2 OSCILLATOR INTERFACE BOARD

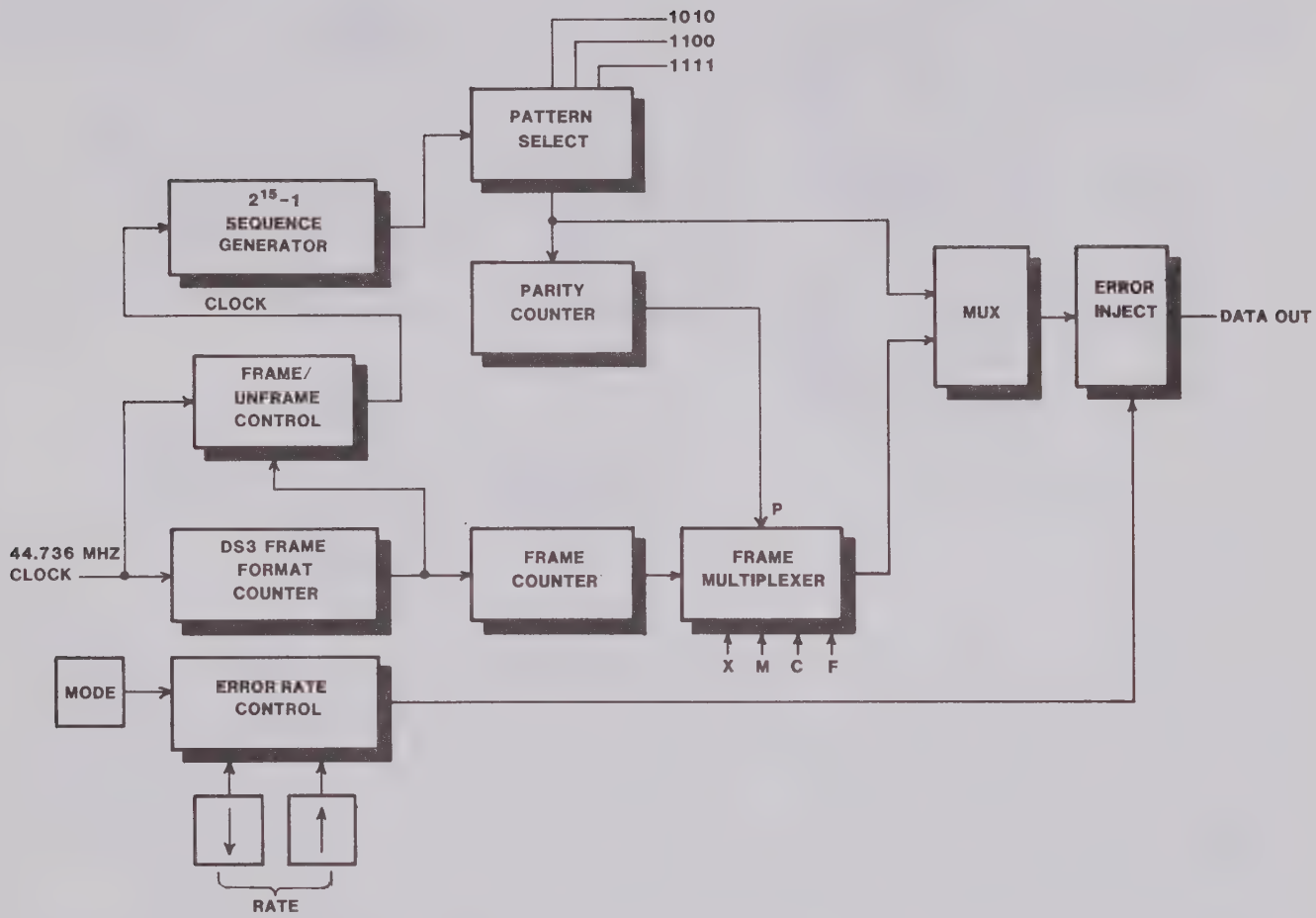


The Oscillator Interface board includes a 44.736MHz crystal-controlled oscillator whose output is fed through an ECL driver circuit to the Transmit Generator board. The Oscillator Interface board also includes circuitry to detect an external clock input applied to the rear-panel EXT CLOCK IN connector. When detected, this circuit switches out the internal oscillator and switches in the external clock signal.

A circuit is included that converts the ECL data and timing signals, from the Transmit Generator board, to NRZ signals. These signals are applied to the front-panel BINARY DATA and CLOCK output connectors.

The M Sync and PR Sync signals from the Transmit Generator board are applied through the Oscillator Interface board to the rear-panel MONITOR connector. The external error-injection signal from the rear-panel ERROR INJECT connector is applied through the Oscillator Interface board to the Transmit Generator board.

7.3 TRANSMIT GENERATOR BOARD



The Transmit Generator board generates the DS3 master-frame data format and the 2^{15}-1 (32,767) bit pseudorandom sequence for bit-error measurements. The board controls both the framed and unframed modes of operation, the insertion of bit errors in the output data format, the pseudorandom sequence, the short patterns (1111,1100,1010), and insertion of the blue signal.

In the unframed mode of operation, the information bits are transmitted without insertion of the DS3 master-frame format. The pseudorandom sequence and the short patterns can be transmitted in the unframed mode of operation by selection of the front-panel PATTERN button and rear-panel Short Pattern switch.

In the framed mode of operation, the DS3 master-frame data bits are inserted into the information bits.

The DS3 format contains 4,760 bits per Master Frame, of which 56 are frame bits. The Transmit Generator generates the proper X,F,C,P, and M frame bits and inserts them into the data pattern.

A 44.2MHz gapped clock is generated so that the pseudorandom sequence operates at the information bit rate. During the gapped output of the sequence, the frame bits are inserted.

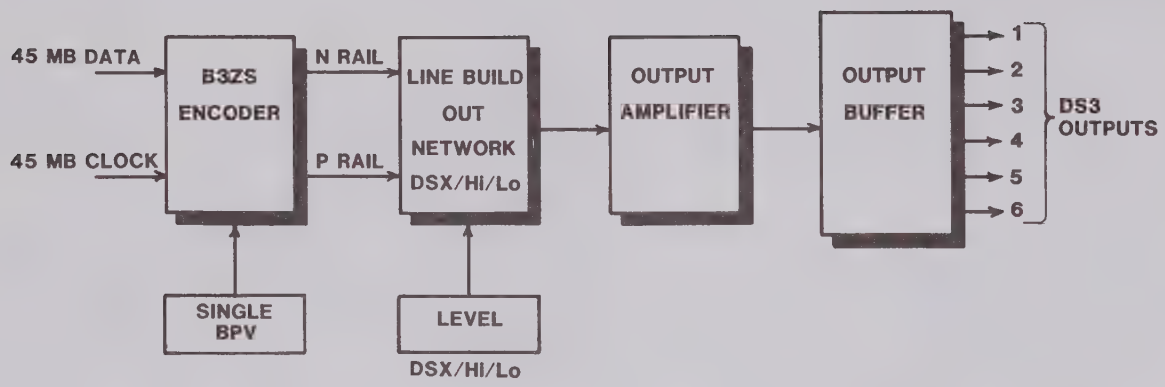
In the framed mode of operation, the Transmit Generator counts all the information bits in the Master Frame. If the digital sum of all 4,704 information bits is 1, the PP frame bits in the next Master Frame are 11. If the sum is 0, PP=00. These are the parity bits in the DS3 format that are used for measuring live traffic in a DS3 transmission system.

The Transmit Generator board includes circuitry to insert bit error-rates of 10^{-9} to 10^{-2} in steps of 10 as set by the front-panel ERROR CONTROL buttons. The errors are inserted in an asynchronous manner so that errors are applied to all bits within the 4,760-bit format. This means that errors are applied to the frame bits as well as the information bits.

In the framed mode, a blue signal can be generated. A blue signal is a 1010 pattern with DS3 frame bits inserted.

The Transmit Generator also generates the PR-Sync and M-Sync pulses. The PR Sync occurs once every 32,767-bit pseudorandom sequence. The M Sync once every 4,760-bit DS3 Master Frame.

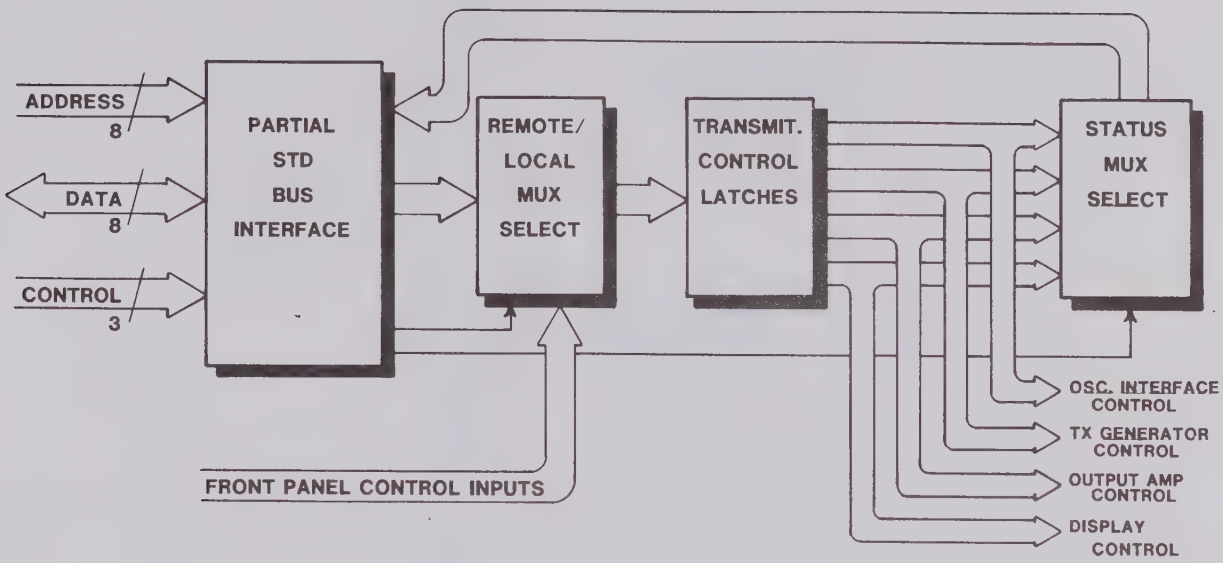
7.4 OUTPUT AMPLIFIER BOARD



The Output Amplifier board converts the NRZ data to B3ZS format, sets the output level of the signal, and inserts single bipolar-pulse-violations in the B3ZS output when the front-panel SINGLE BPV error button is pushed.

The binary NRZ data and the timing information from the Transmit Generator are applied to the B3ZS encoder on the Output Amplifier board. Two RZ rails are generated by the B3ZS encoder, a P rail and an N rail. These two rails are combined and amplified, sent through a pulse amplifier, and applied to a line-build-out network. There are three sections of this network (high, DSX, and low) which are selected by the front-panel LEVEL button. DSX builds out 450 feet of cable, High is straight through, and Low builds out a 13.8 dB pad. The output of the amplitude-and-line-build-out network is fed to an output driver that drives six output buffers, each of which is connected to one of the six DS3 OUTPUT connectors on the front panel.

7.5 STD INTERFACE BOARD



The STD Interface board provides 1-of-2 switching between GPIB software control of the S5200D transmitter and local front-panel control.

When the GPIB option is installed and a GPIB controller has requested remote control of the transmitter, all front-panel control inputs are switched out and the software control inputs are switched in. A partial STD bus interface allows the CPU board to issue transmitter commands and read transmitter status. Front-panel inputs are conveyed to this board by a flat ribbon cable interface from the front-panel printed circuit assembly. Transmitter control outputs from this board are conveyed to the Transmit Generator and Oscillator-Interface boards by a non-standard transmitter control and status bus. Status inputs from these boards and the rear panel are provided over this same bus.

When the GPIB option is not installed, the 1-of-2 switching is disabled and local front-panel control is permanently enabled.

STD Bus	Description	Pin	Description	Pin
	Address		Processor Control (cont)	
	A0 thru A15	15 thru 30	MEMEX' (unused)	36
			REFRESH'	37
	Data		MCSYNC'(unused)	38
	D0 thru D7	7 thru 14	M1'	39
			STATUS 0' (unused)	40

Power & Ground

+5V.....1,2
Ground.....3,4
-5V.....5,6
Auxiliary ground.....53,54
+12V (unused).....55
-12V (unused).....56

Processor Control

WR'.....31
RD'.....32
IORQ'.....33
MEMRQ'.....34
IOEXP' (unused).....35

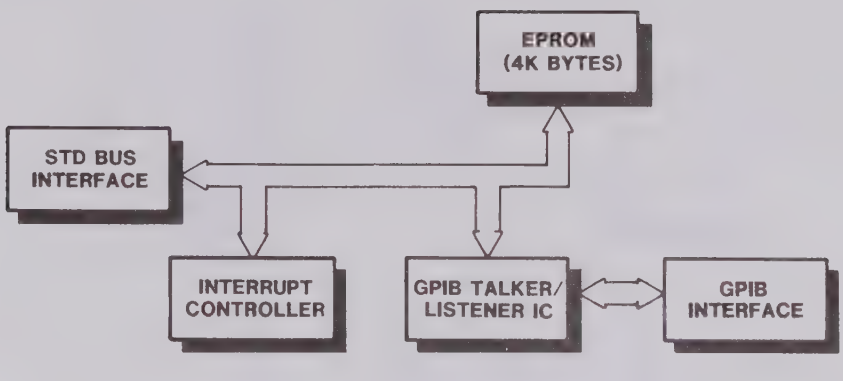
BUSAK'.....41
BUSRQ'.....42
INTAK'.....43
INTRQ'.....44
WAITRQ'.....45

NMIRQ'.....46
SYSRESET'.....47
PRRESET'.....48
CLOCK'.....49
CNTRL' (unused).....50

PCO'.....51
PCI.....52

NOTE WR' implies active low signal.

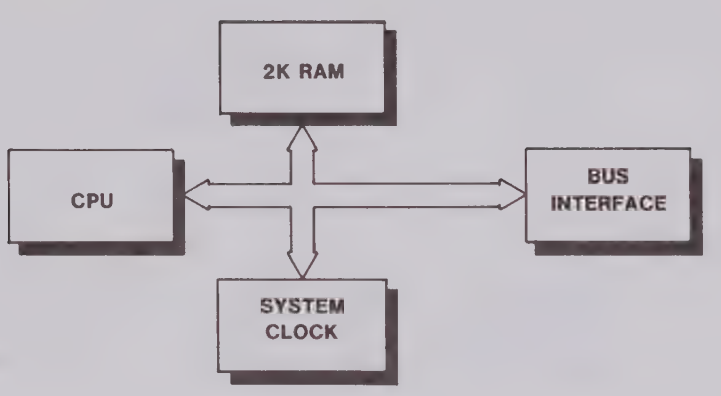
7.6 GPIB BOARD



The GPIB board provides an interface between the STD bus and IEEE-488 interface. Most of the interfacing is handled automatically by an Intel 40-pin LSI device. GPIB activity causes status bits to be set in this IC which generates an interrupt to alert the CPU that something has happened. The CPU reads status and data from the GPIB IC and determines what software action to take.

When GPIB commands are received by the GPIB Board and processed by the CPU, the CPU writes the output to the GPIB IC. The GPIB IC controls the output on a byte-by-byte basis.

7.7 CPU BOARD

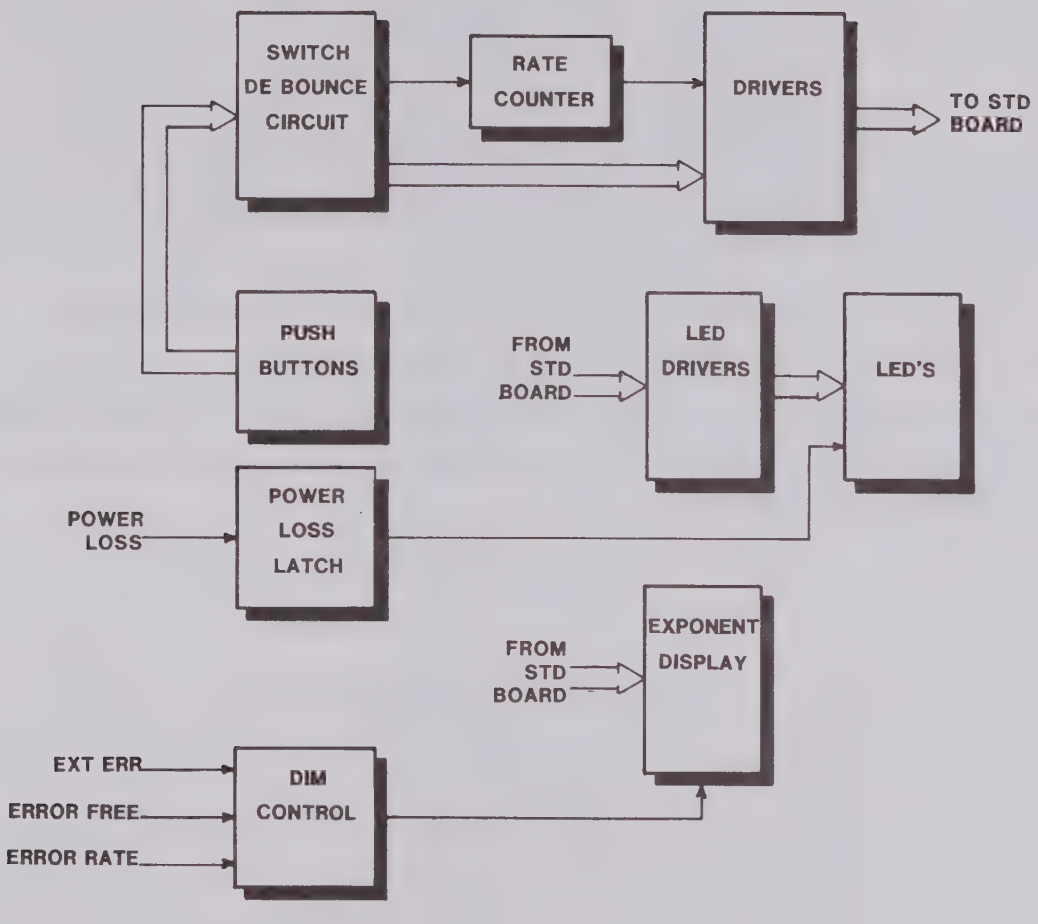


This board contains a Z80 microprocessor, 2K (2048) bytes of volatile static RAM, and the interface circuitry necessary for compatibility with the 56-pin STD bus.

The Z80 microprocessor is a 40-pin LSI device capable of addressing 65K bytes of memory and 256 I/O ports. It operates on 8-bit parallel data.

The 2048 bytes of RAM provide read/write storage for transmitter software variables and stack operations. Included in this RAM is a 512 byte GPIB output queue and a 128 byte GPIB input command buffer.

7.8 FRONT-PANEL DISPLAY BOARD



The front-panel display board consists of pushbutton controls, LED's and circuitry to interface these controls and LED's to the plug-in printed circuit boards and to control the functions and display the status of the transmitter.

All pushbuttons go through a switch debounce circuit. So, when any button is pushed, a single pulse is generated.

The LEVEL button output drives a divide by 3 counter which generates two outputs to control the transmit levels DSX, HI, and LO.

The FRAME/UNFRAMED and PATTERN button drives a divide by 2 circuit whose output is fed to the STD plug in the board where it controls the frame and pattern select functions.

The MODE button output drives a divide by 3 counter which has three outputs to control the ERROR FREE, ERROR RATE, and EXTERNAL error modes of operation.

The RATE up and down buttons control a BCD up/down counter on the front-panel display board. When the down button is pushed, the counter counts up to indicate a lower bit error-rate, and when the up button is pushed, the counter counts down to indicate a higher bit error-rate. The BCD outputs of the counter are FED through the STD plug-in card to the transmit generator card where it controls the insertion of errors into the output data.

The single BPV and bit pushbutton outputs feed through the STD card to the transmit generator to control the single error insertion.

Also located on the display panel is the power loss latch. When power is lost and regained, the loss latch is set and turns on the power loss LED. The latch is reset by the RESET/LED TEST button.

7.9 SOFTWARE THEORY OF OPERATION

When the GPIB option is installed, two software-control functions are provided: power-up self-test and GPIB remote control.

Power-up Self-Test

On power-up the software takes control very briefly to perform a basic self-test. All system RAM, program PROM, and remote/local switching control is tested. If any failures are detected during this self-test, a failure code is displayed for 5 seconds in the ERROR RATE LED. See Section 8, Service, for a list of failure codes and interpretation.

After the 5-second failure-code display, the software will again attempt a reinitialization and self-test. If the failure persists, the software will repeat this cycle ad infinitum.

If no failures are found, the self-test ends in less than 2 seconds and the S5200D transmitter is initialized under local front-panel control.

GPIB Control

The reception of GPIB commands "wakes up" the software. When the transmitter is commanded to remote mode by GPIB, the software takes control of the transmitter functions. GPIB control software interprets incoming commands and outputs appropriate transmitter hardware control signals. Query commands cause the software to read transmitter hardware status and format ASCII output messages. These messages output to the GPIB hardware one character at a time.

Section 8, Service

8.1 ASSISTANCE

For service assistance call the Tau-Tron Customer Service Dept., (617)256-9013. Their experience and expertise can often save you valuable time in correcting any equipment Malfunction.

8.2 REPAIR RETURNS

To return a unit for repair:

1. Call the Customer Service Dept., (617)256-9013, for a Repair Authorization Number. This will reduce administrative delays and ensure prompt return of your unit.
2. Complete and attach the Repair Tag, in the rear of the manual, to your unit for positive identification.
3. Pack the unit in the original shipping carton and packing materials, if available. Otherwise use a double-walled carton (test strength of 350lb) and pack securely to prevent any movement in the carton during transit. Secure the carton by sealing with heavy paper tape.
4. Send to : Tau-Tron
   27 Industrial Ave.
   Chelmsford, MA 01824
   Attn: Customer Service

8.3 ROUTINE SERVICE

WARNING Do not attempt access to rear-panel air filter without disconnecting the line cord from the power receptacle.

Air Filter Periodically clean the rear-panel air filter to maintain proper air flow for adequate cooling:

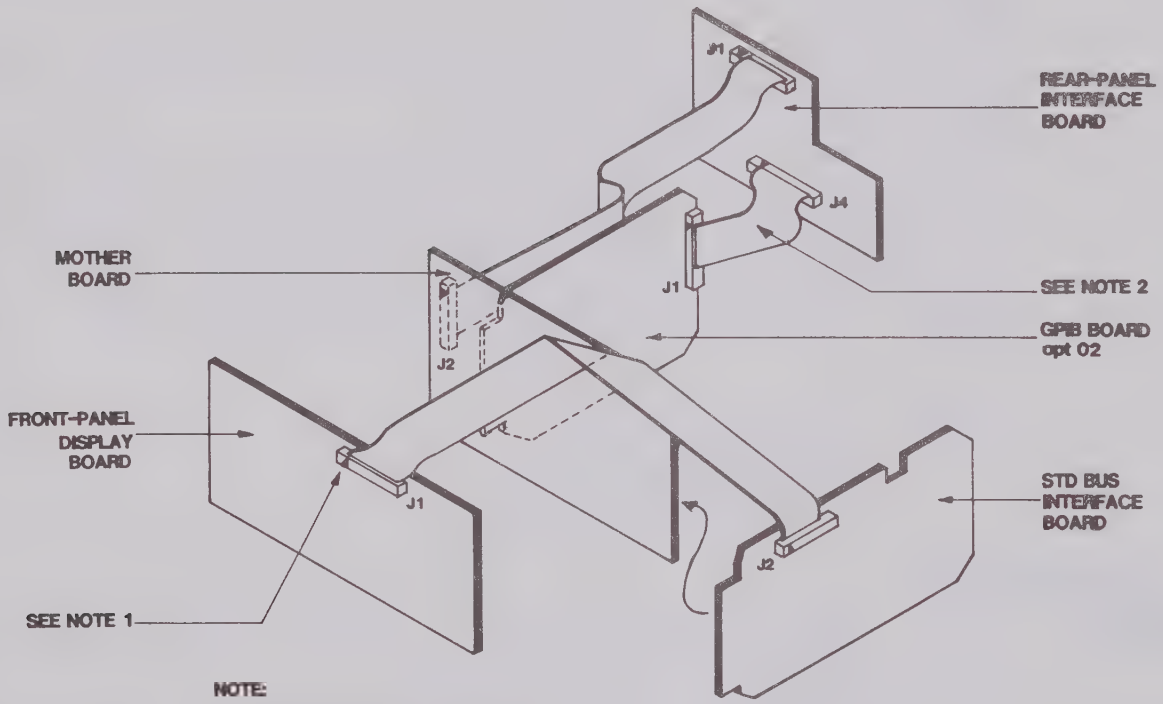
1. Remove the two slot-head screws from the filter holder and remove the holder and sponge-rubber filter.
2. Use a vacuum cleaner to clean the filter.
3. Reinstall the filter and holder and secure with the two screws.

8.4 GENERAL TROUBLESHOOTING

WARNING Hazardous voltages exist in this equipment. Stay clear of all line-voltage wiring and terminals.

Board and Connector Seating

Be sure all printed circuit boards are securely seated in their connectors. Be sure the hold down bracket is tightly secured. Be sure interconnecting ribbon cables are properly secured as shown in the drawing.



NOTE:

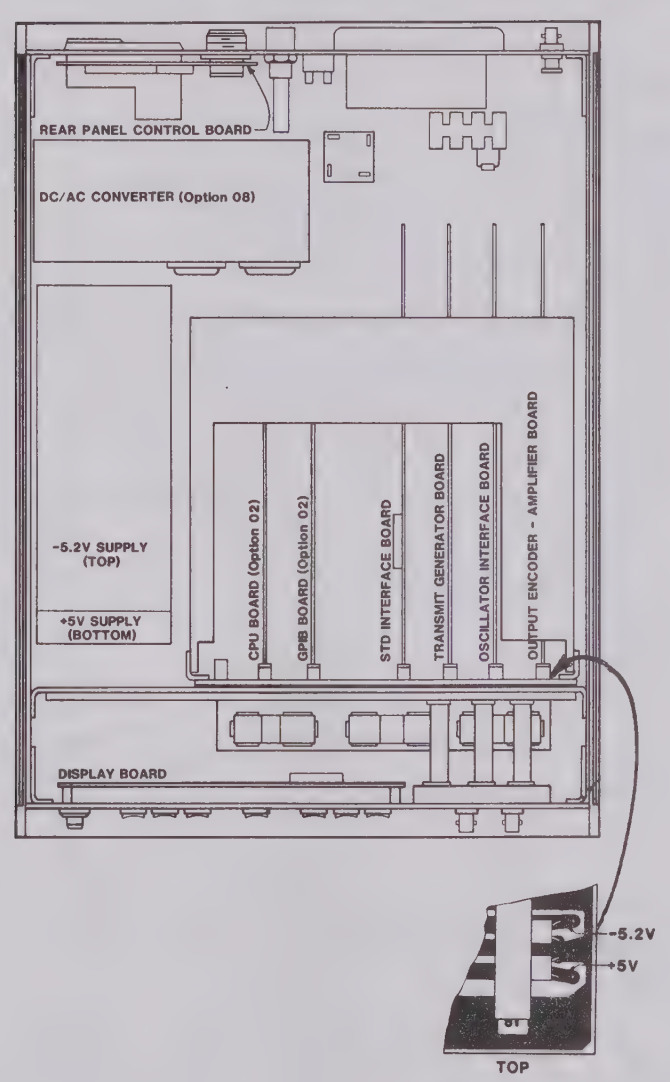
1. ▲ DENOTES PIN 1.
2. THIS CABLE IS A 40 CONNECTOR, OTHER CABLES ARE 26 CONNECTOR.

FLAT RIBBON CABLE INTERCONNECTIONS

DC Voltages

Check the power-supply outputs as follows:

+5V ±0.2V
-5.2V ±0.2V



Nicad Battery

A 1.2V Nickel Cadium battery pack is used in the transmitter to preserve front-panel settings in case of a power failure. If the battery is discharged or disconnected, the front-panel power up conditions will be incorrect.

Visual access to the battery pack may be gained by removing the top cover.

The battery type is General Electric KØ1H111C-GT1.

8.5 SOFTWARE DIAGNOSTICS

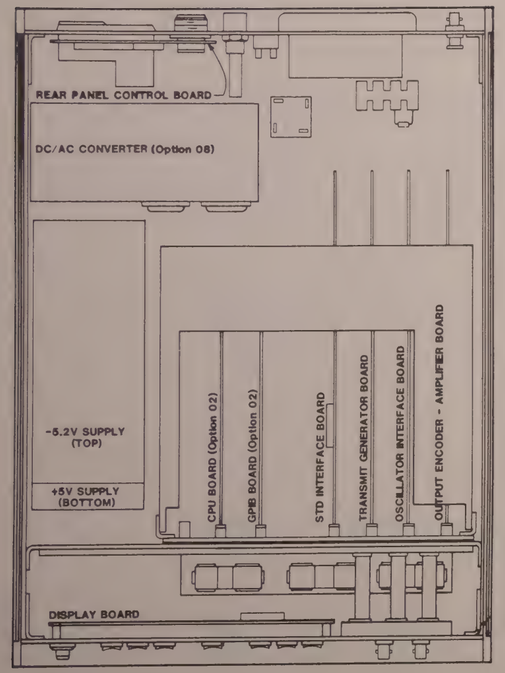
With OP-02, IEEE-488 Interface, software briefly takes control to perform a basic self-test. All system RAM, program PROM, and remote/local switching control is tested. If any failures are detected during this self-test, a flashing failure code is displayed for 5 seconds in the ERROR RATE LED, as follows:

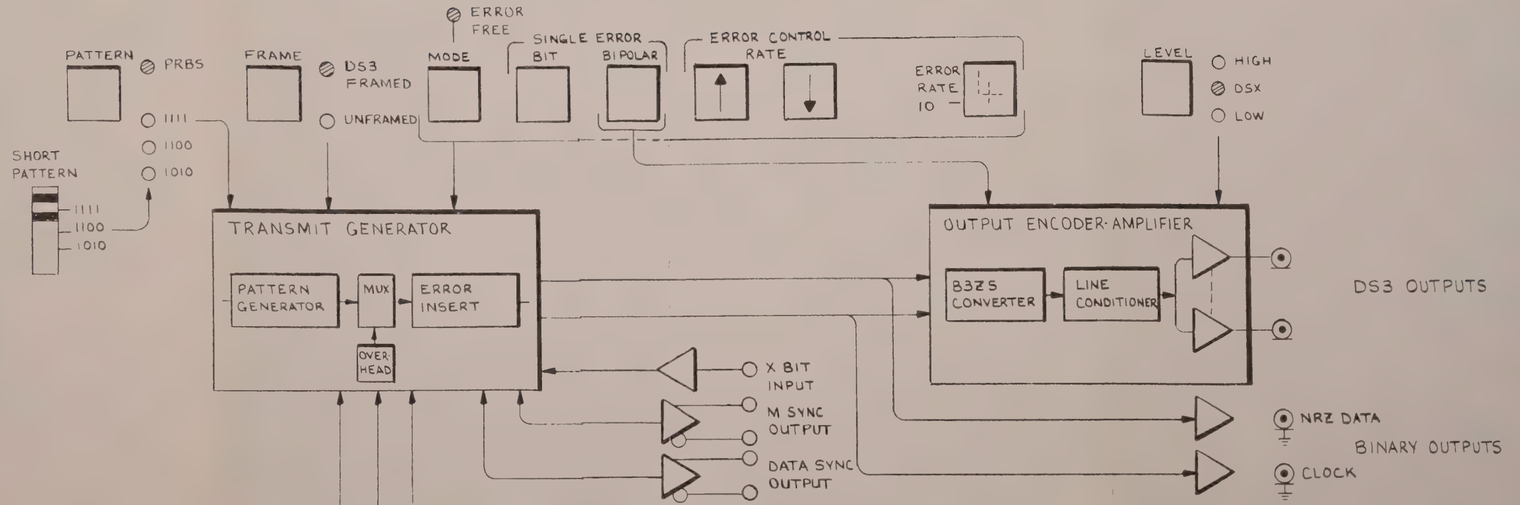
Failure Code	Meaning
0	Bad RAM at U11 on CPU board.
1	Bad EPROM at U12 on GPIB board.
2	Bad EPROM at U15 on GPIB board.
3	Bad EPROM at U19 on GPIB board.
4	Error trying to software-control the S5200D transmitter.
5	Error returning S5200D transmitter to local control.
6	GPIB addressed to talk and listen simultaneously.
7	Software queue problem.
8	Interrupt generated by an unused interrupt-controller channel.
9	Invalid memory access.
A thru F	Undefined.

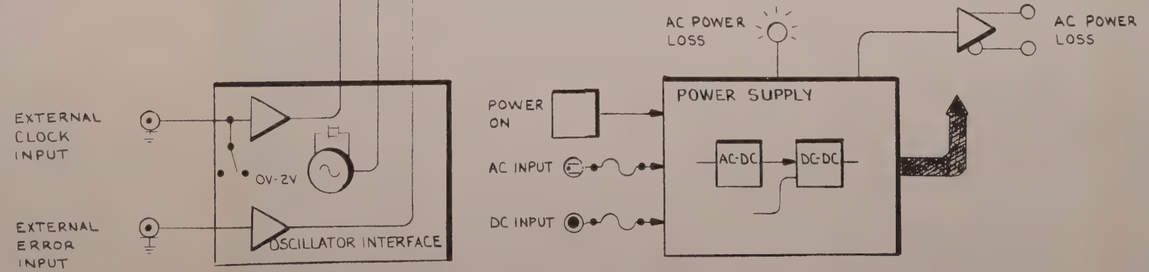
After the 5-second failure-code display, the software will again attempt a reinitialization and self-test. If the failure persists, the software will repeat this cycle ad infinitum. Under these conditions, the S5200D transmitter cannot be remotely controlled.

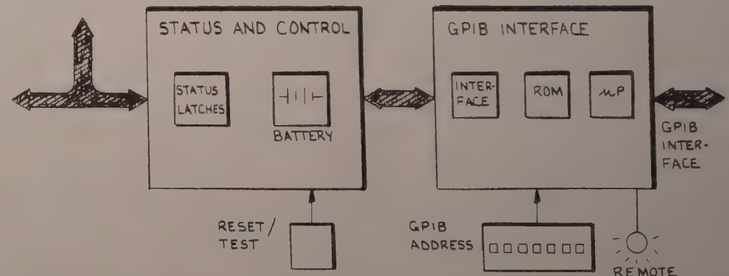
If no failures are found, the self-test ends in less than 2 seconds and the S5200D transmitter is initialized under local front-panel control.

Section 9, Diagrams









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2. Complete and **attach one of the Repair Tags** below to your unit.
3. **Pack the unit** in the original shipping carton and packaging materials, if available. Otherwise use a double-walled carton (test strength of 350 lb) and shock absorbing material such as bubble wrap to prevent the unit from moving in the carton during transit. Seal with heavy paper tape.
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   Westford, MA 01886
   attn: Customer Service

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Model _____ **Serial Number** _____

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Model _____ **Serial Number** _____

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